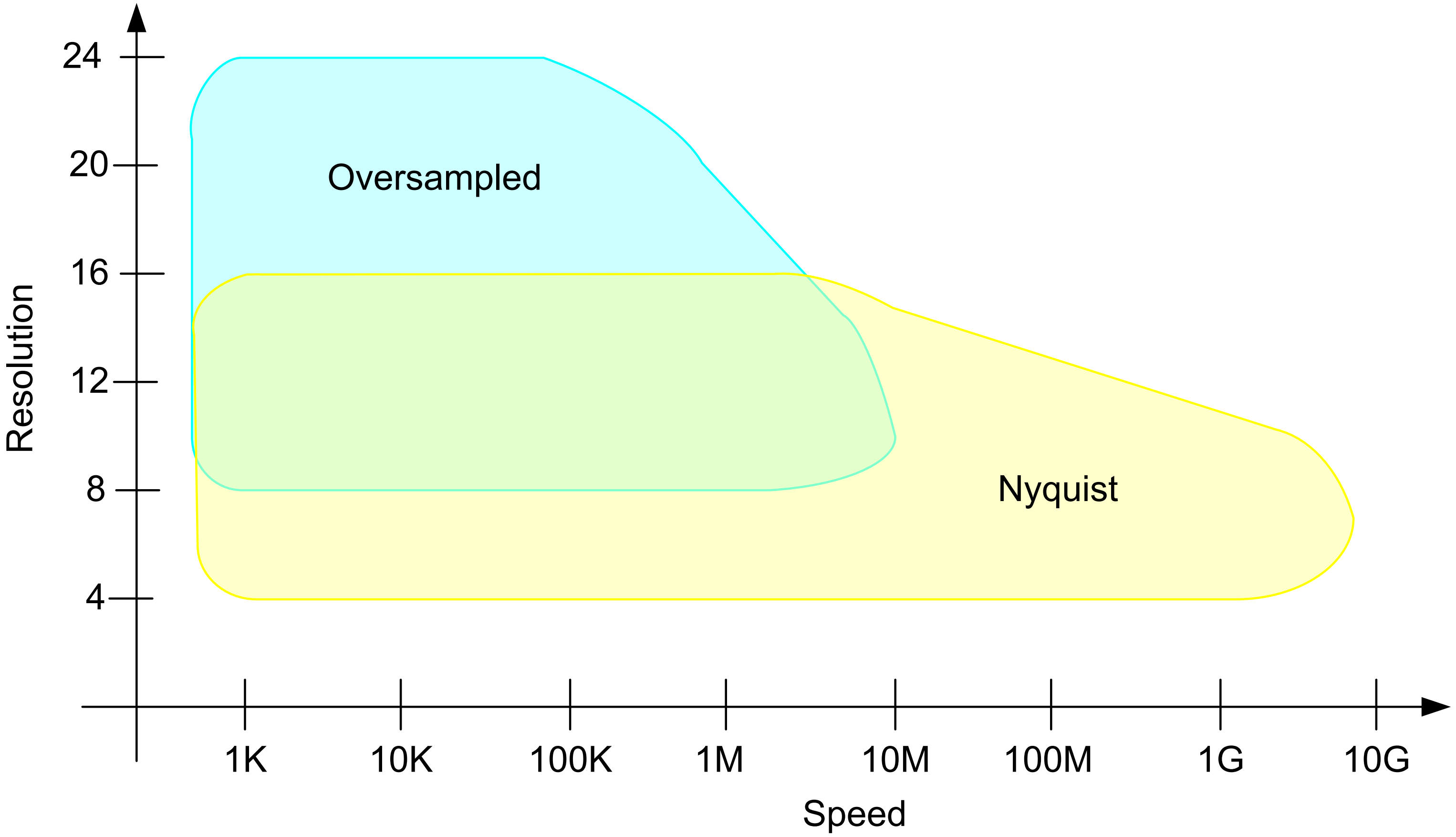
# EE 505

## Lecture 26

## Oversampled ADCs
## Layout of Matching Critical Components

# Data Converter Type Chart

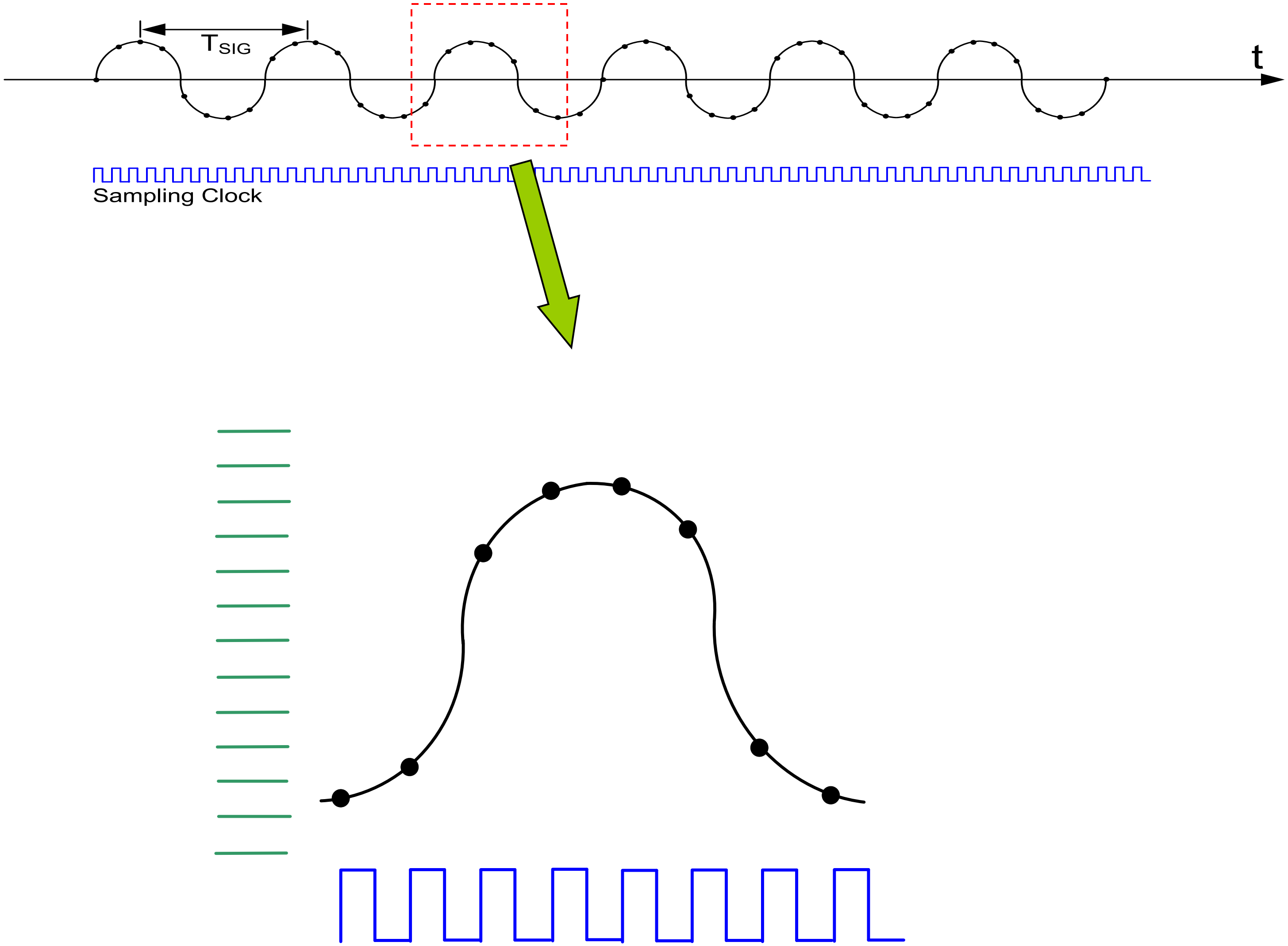


# Over-Sampled Data Converters

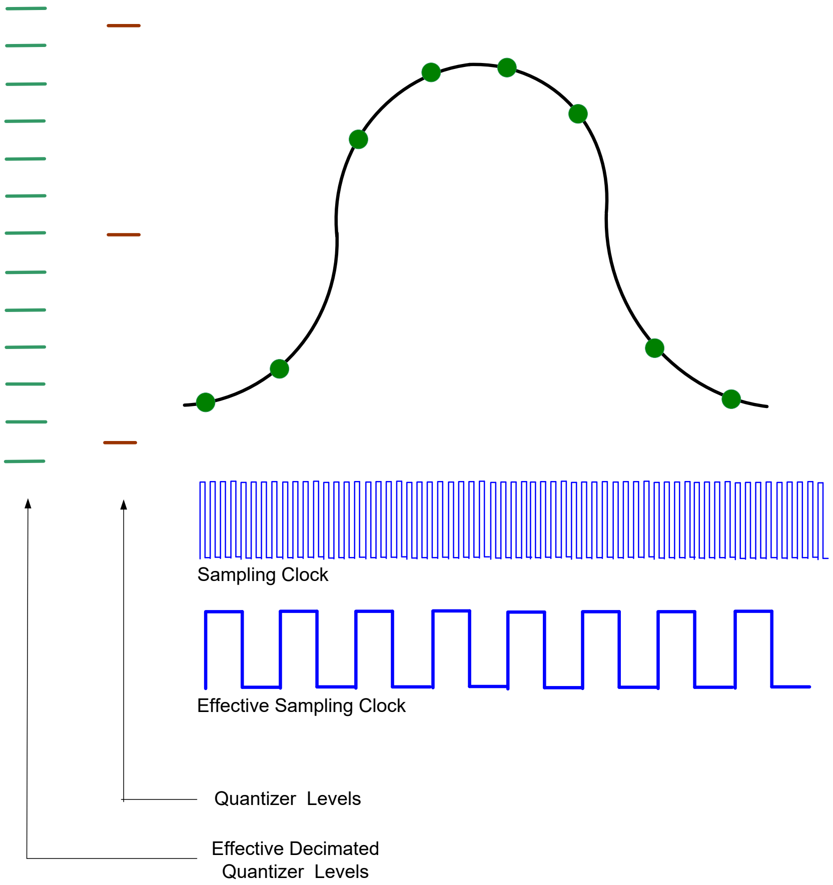
## General Classes

- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time

# Nyquist Rate



# Over-Sampled



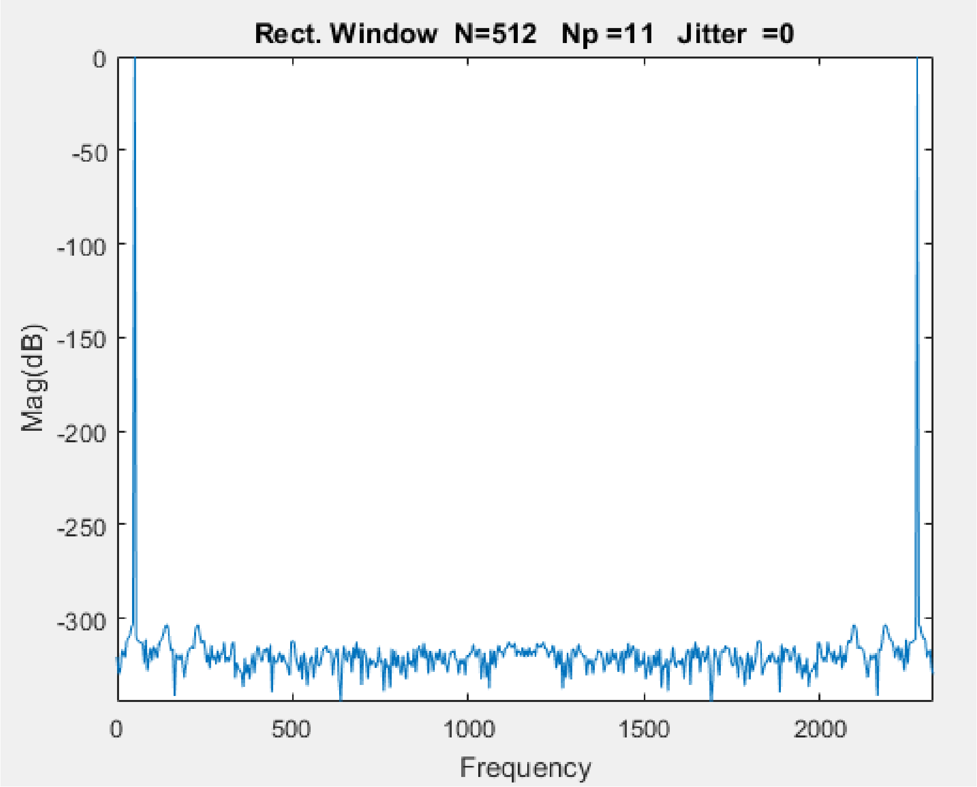
Over-sampling ratios of 128:1 or 64:1 are common

Dramatic reduction in quantization noise effects

Limited to relatively low frequencies

# Recall with no quantization:

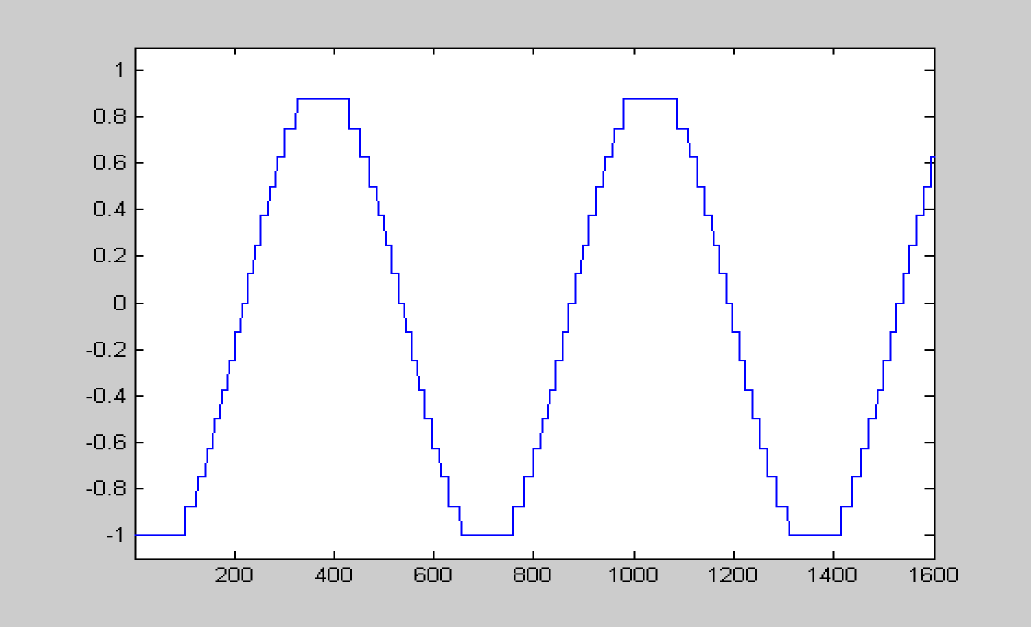
$f_{SIG}$=50Hz
$f_{NYQ}$=100Hz
$f_{SAMP}$=2.3KHz
Oversampled: 23:1



MatLab Results

Recall:

# Quantization Effects



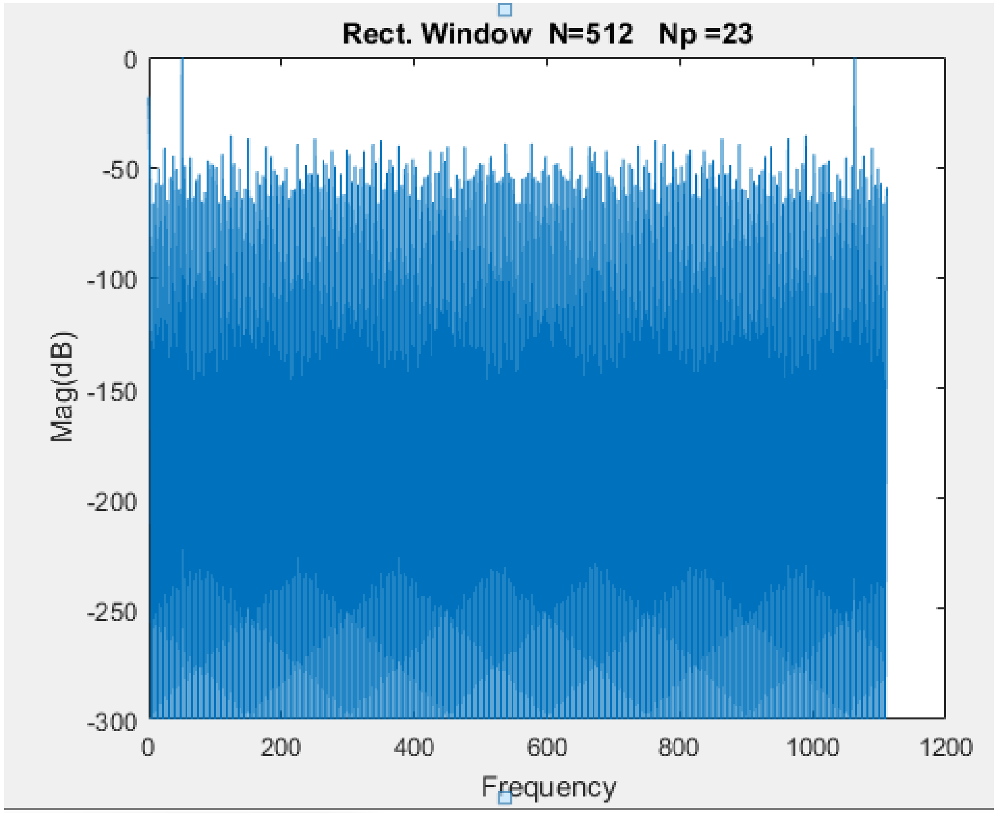
**Simulation environment:**

$N_P$=23
$f_{SIG}$=50Hz

Recall:

# Quantization Effects

Res = 4 bits



$f_{SIG}$=50Hz
$f_{NYQ}$=100Hz
$f_{SAMP}$=1113KHz
Oversampled: 11:1

RMS Quantization Noise:

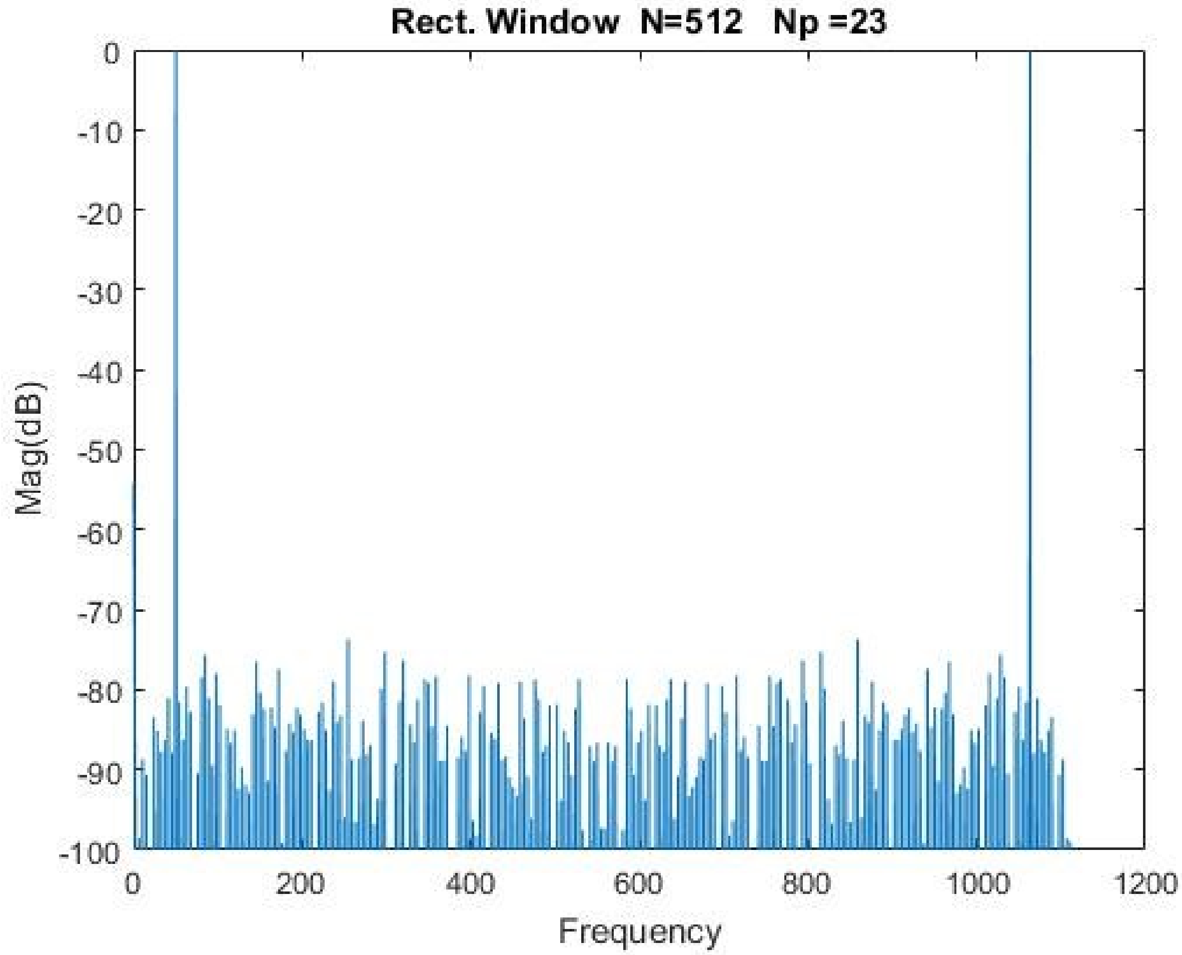
$$E_{RMS} = \frac{x_{LSB}}{\sqrt{12}}$$

**Lets now increase resolution**

Recall:

# Quantization Effects

Res = 10 bits



$f_{SIG}$=50Hz
$f_{NYQ}$=100Hz
$f_{SAMP}$=1113KHz
Oversampled: 11:1

$$E_{RMS} = \frac{x_{LSB}}{\sqrt{12}}$$

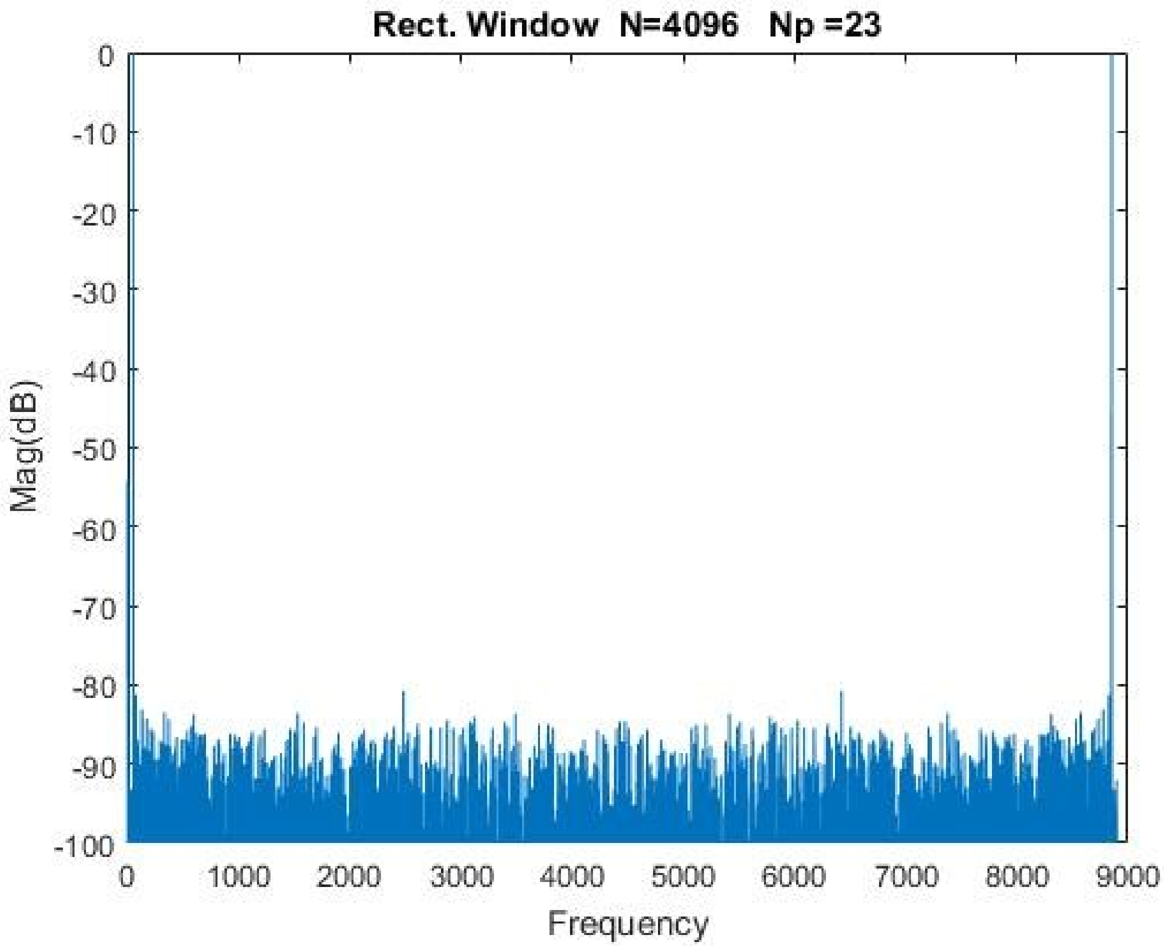
Quantization noise is much lower but still significant

**Lets now increase oversampling ratio (i.e. number of samples)**

Recall:

# Quantization Effects

Res = 10 bits



$f_{SIG}$=50Hz
$f_{NYQ}$=100Hz
$f_{SAMP}$=8904KHz
Oversampled: 89:1

$$E_{RMS} = \frac{x_{LSB}}{\sqrt{12}}$$

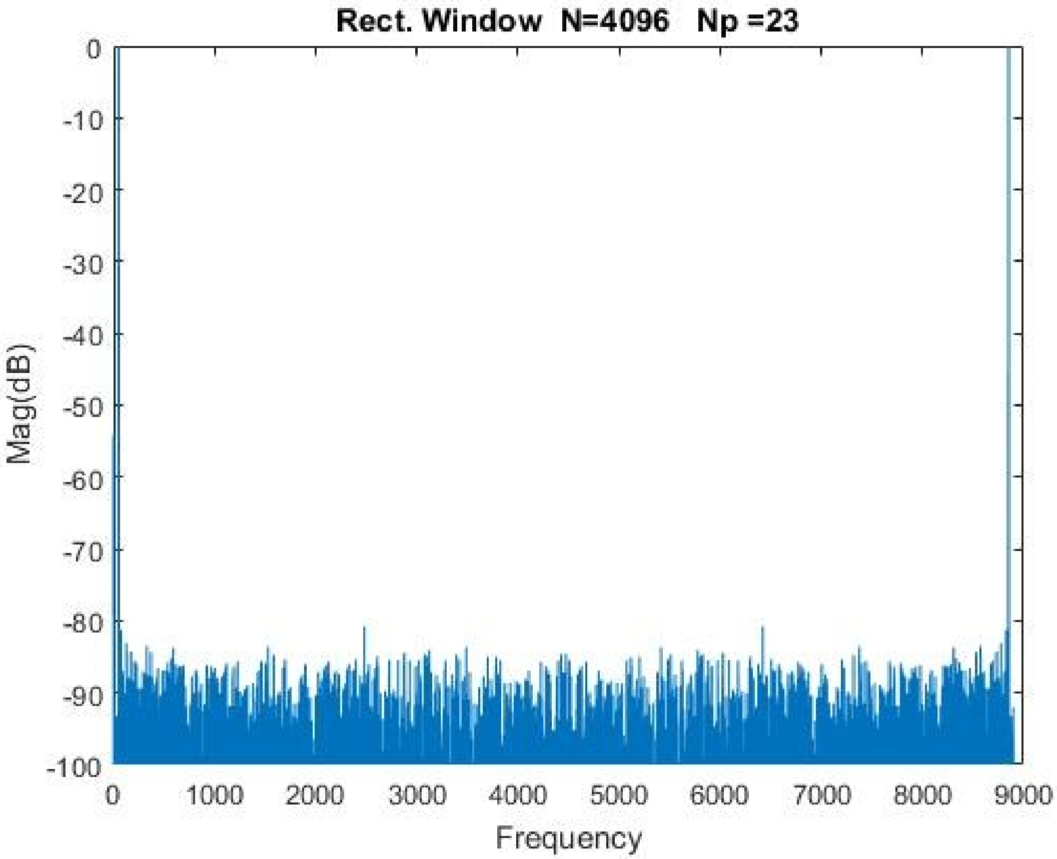
Compared to the previous slide, it appears that the quantization noise has gone down

But has it ? Magnitude of quantization DFT terms decreased but $E_{RMS}$ unchanged

Recall:

# Quantization Effects

Res = 10 bits

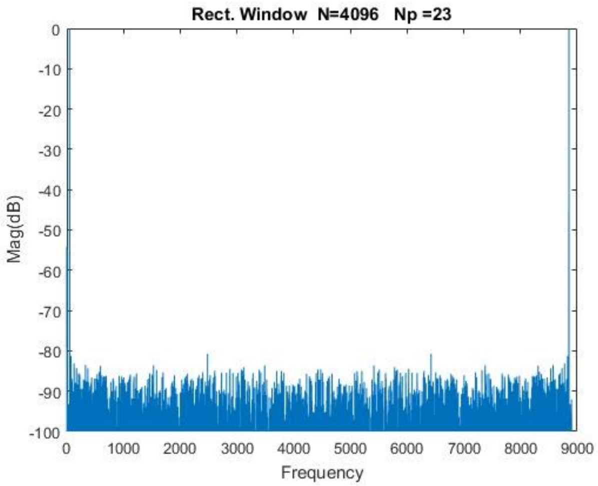


$f_{SIG}$=50Hz
$f_{NYQ}$=100Hz
$f_{SAMP}$=8904KHz
Oversampled: 89:1

$$E_{RMS} = \frac{x_{LSB}}{\sqrt{12}}$$

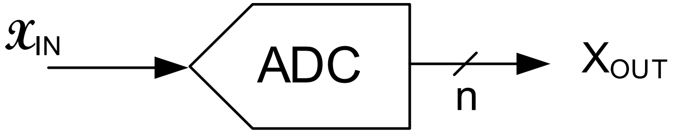
Can any additional useful information about the input be obtained since we have many more samples than are needed?

# Over-Sampling



Res = 10 bits

$f_{SIG}$=50Hz
$f_{NYQ}$=100Hz
$f_{SAMP}$=8904KHz
Oversampled: 89:1



$$E_{RMS} = \frac{x_{LSB}}{\sqrt{12}}$$

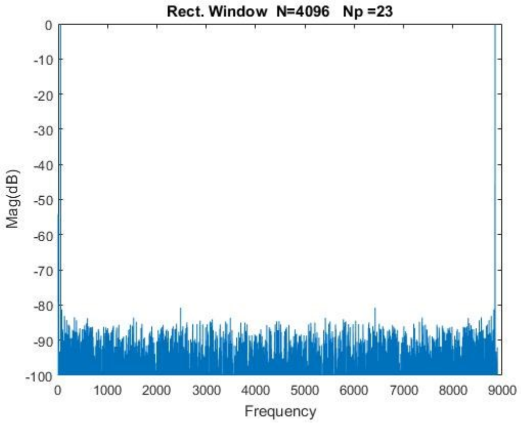
What would happen if we break the 4096 samples into groups of 20 samples and form?

$$\hat{X}_{OUT}(k \bullet 20T_{SAMP}) = \frac{1}{20}\sum_{j=1}^{20} x_{OUT}\left(jT_{SAMP} + 20kT_{SAMP}\right)$$

$$E_{RMS} = ?$$

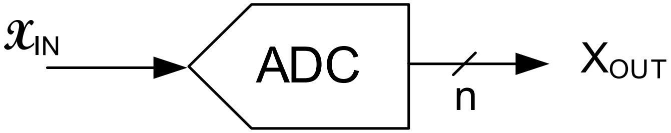
- Though the individual samples have been quantized to 10 bits, the arithmetic operations will have many more bits
- The effective sampling rate has been reduced by a factor of 20 but is still over 4 times the Nyquist rate
- Has the quantization noise been reduced (or equivalently has the resolution of the ADC been improved?
- Is there more information available about the signal?

# Over-Sampling



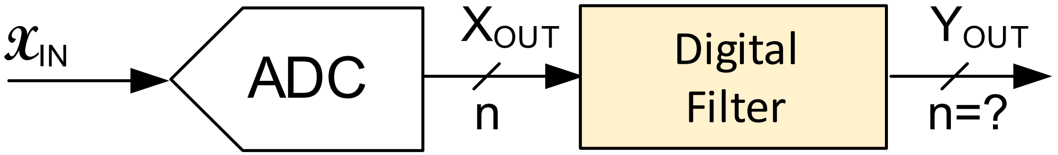
Res = 10 bits

$f_{SIG}$=50Hz
$f_{NYQ}$=100Hz
$f_{SAMP}$=8904KHz
Oversampled: 89:1



$$E_{RMS} = \frac{x_{LSB}}{\sqrt{12}}$$

Since the quantization noise is at high frequencies, what would happen if filtered the Boolean output signal?

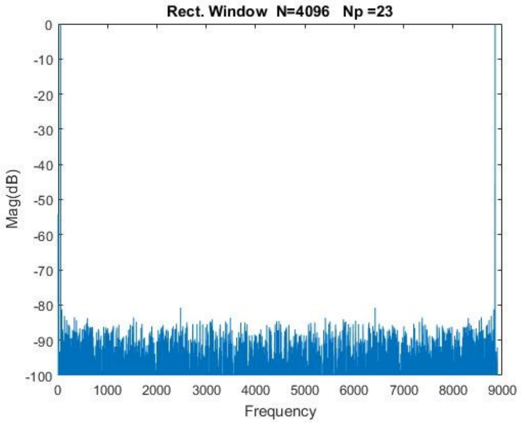


$$E_{RMS} = ?$$

$$Y_{OUT}(kT_{SAMP}) = \sum_{j=0}^{m} a_j x_{OUT}\left(k - jT_{SAMP}\right)$$

Or $$Y_{OUT}(kT_{SAMP}) = \sum_{j=0}^{m} a_j x_{OUT}\left(k - jT_{SAMP}\right) + \sum_{j=1}^{h} b_j Y_{OUT}\left(k - jT_{SAMP}\right)$$

# Over-Sampling



Res = 10 bits

$f_{SIG}$=50Hz
$f_{NYQ}$=100Hz
$f_{SAMP}$=8904KHz
Oversampled: 89:1

$$E_{RMS} = \frac{x_{LSB}}{\sqrt{12}}$$

What does this difference equation represent?

$$Y_{OUT}(kT_{SAMP}) = \sum_{j=0}^{m} a_j x_{OUT}\left(k - jT_{SAMP}\right)$$

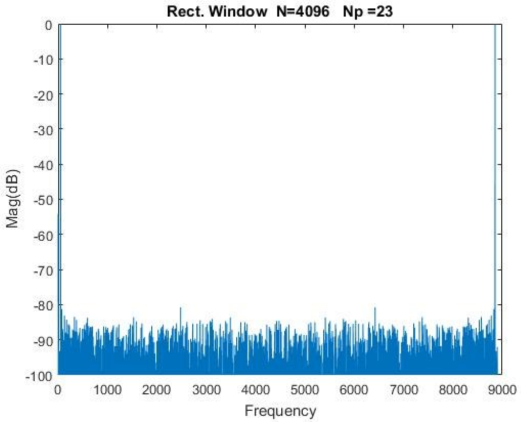
- Moving Average (MA) Digital Filter ⟺ $H(z) = \sum_{i=1}^{m} a_i z^i$
- Filter shape (e.g. low-pass, band-pass, high-pass, … dependent upon $<a_i>$ coefficients)

What does this difference equation represent?

$$Y_{OUT}(kT_{SAMP}) = \sum_{j=0}^{m} a_j x_{OUT}\left(k - jT_{SAMP}\right) + \sum_{j=1}^{h} b_j Y_{OUT}\left(k - jT_{SAMP}\right)$$

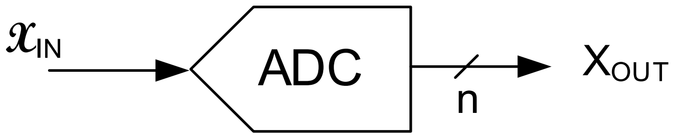
- Auto Regressive Moving Average (ARMA) Digital Filter ⟺ $H(z) = \frac{\sum_{i=1}^{m} a_i z^i}{\sum_{i=0}^{n} b_i z^i}$
- Filter shape (e.g. low-pass, band-pass, high-pass, … dependent upon $<a_i>$ and $<b_j>$ coefficients)

# Over-Sampling



Res = 10 bits

$f_{SIG}$=50Hz
$f_{NYQ}$=100Hz
$f_{SAMP}$=8904KHz
Oversampled: 89:1

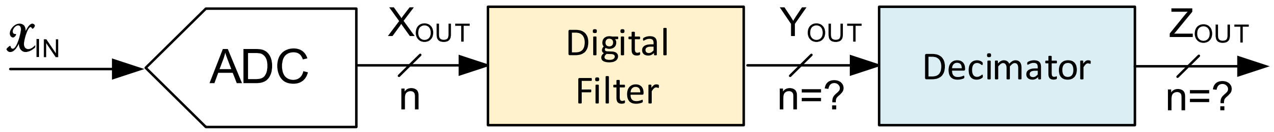


$$E_{RMS} = \frac{x_{LSB}}{\sqrt{12}}$$

Since the quantization noise is at high frequencies, what would happen if filtered and decimated the Boolean output signal?

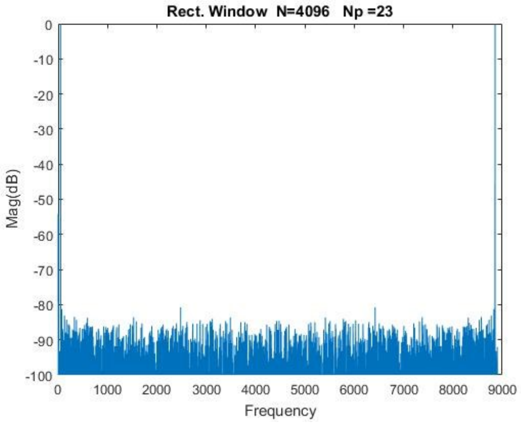
$$Y_{OUT}(kT_{SAMP}) = \sum_{j=0}^{m} a_j x_{OUT}(k - jT_{SAMP})$$

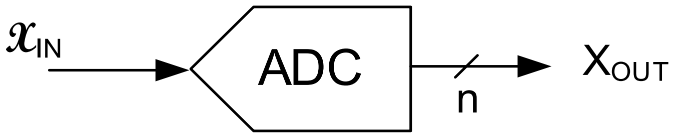
$$Y_{OUT}(kT_{SAMP}) = \sum_{j=0}^{m} a_j x_{OUT}(k - jT_{SAMP}) + \sum_{j=1}^{h} b_j Y_{OUT}(k - jT_{SAMP})$$



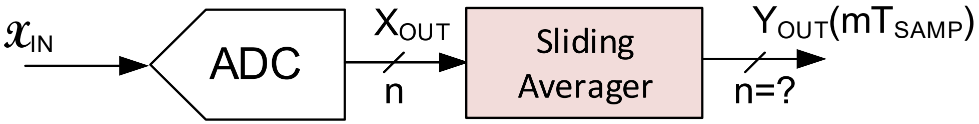
$$E_{RMS} = ?$$

# Over-Sampling

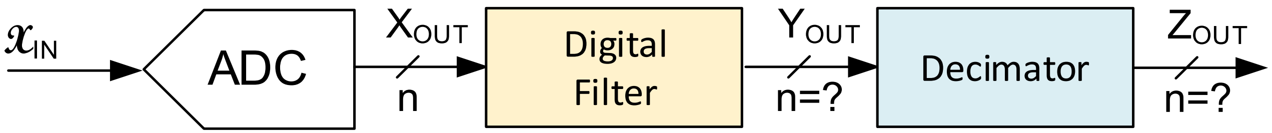




$$E_{RMS} = \frac{x_{LSB}}{\sqrt{12}}$$



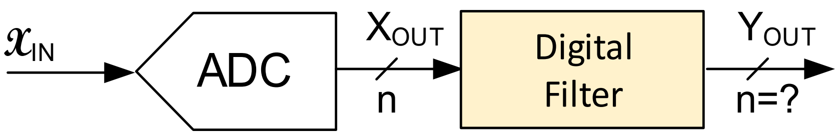
$$E_{RMS} = ?$$



$$E_{RMS} = ?$$

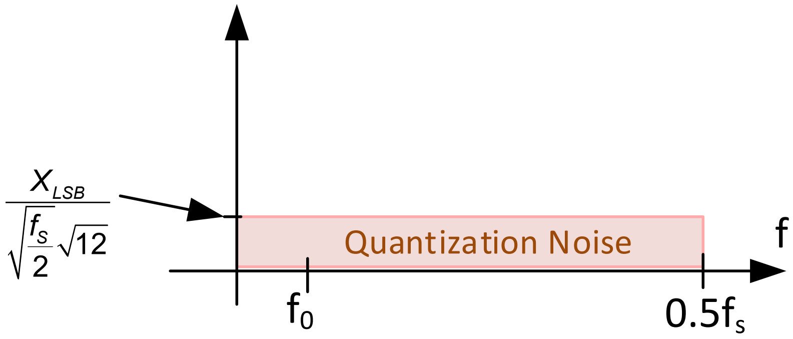
- What is the overhead?
- What is the performance potential?
- How can these or related over-sampling approaches be designed?
- Though this approach may help quantization noise, will not improve ADC linearity

# Over-Sampling



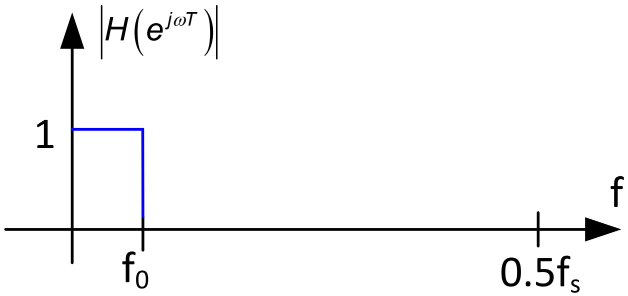
$f_S=f_{SAMP}$

$$OSR=\frac{f_S}{2}\frac{1}{f_0}$$



With ideal lowpass filter with band-edge at $f_0$

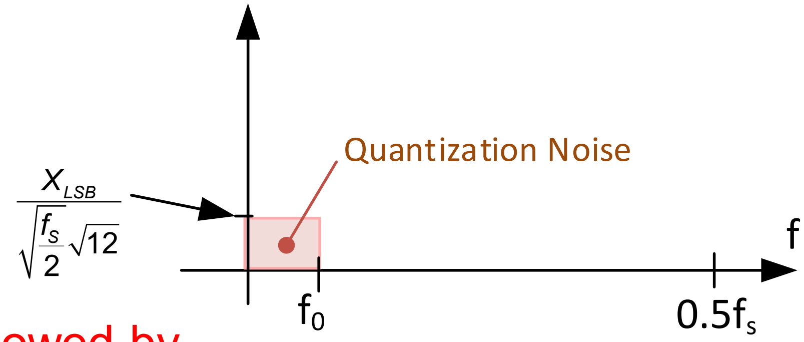
$$V_{Qrms}=\frac{V_{LSB}}{\sqrt{12}}\frac{1}{\sqrt{OSR}}$$



For sinusoidal input with p-p value $V_{REF}$

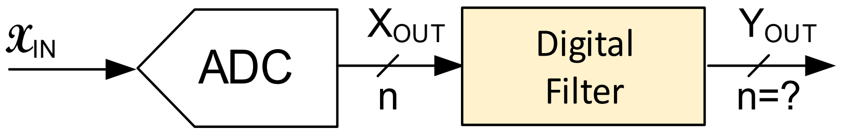
$$SNR=6.02n+1.76+10\log(OSR)$$

Improvement of 3dB/octave or 0.5bits/octave

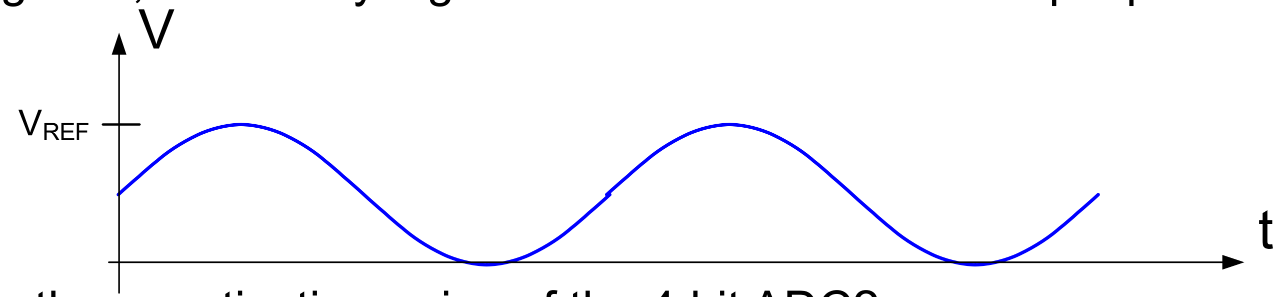


Oversampling increases resolution and if followed by LP filter Reduces Quantization Noise!

# Over-Sampling



Example: If we sample a sinusoidal waveform at a rate of 1000 samples/period with a 4-bit ADC and at each time we create a 16-point moving sum, how many digits will we have at each sample point?



What is the quantization noise of the 4-bit ADC?

$$V_{n\_RMS} = \frac{V_{LSB\_4}}{\sqrt{12}} = \frac{V_{REF}}{2^4\sqrt{12}} = \frac{V_{REF}}{2^5\sqrt{3}}$$

Have we created an 8-bit ADC by simply over sampling?

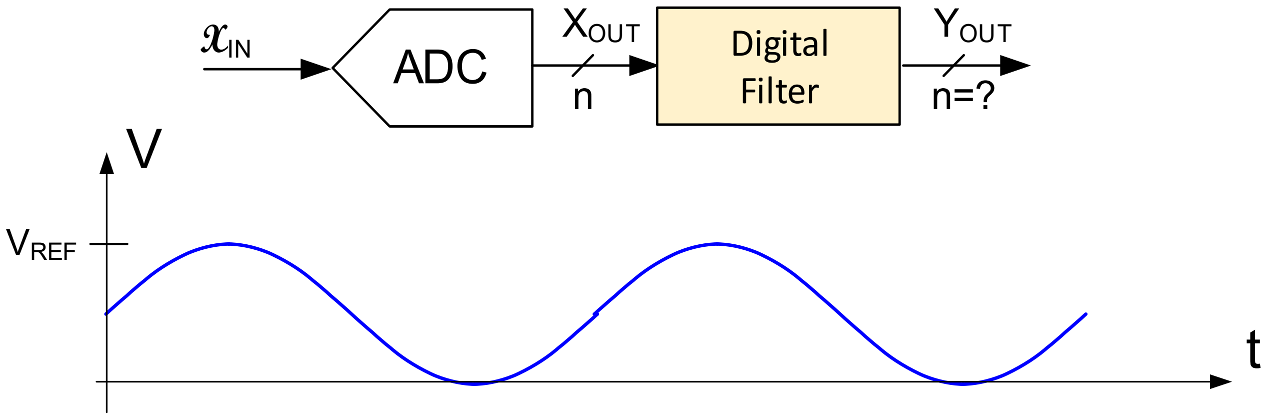
What is the quantization noise of an 8-bit ADC?

$$V_{n\_RMS} = \frac{V_{LSB\_8}}{\sqrt{12}} = \frac{V_{REF}}{2^8\sqrt{12}} = \frac{V_{REF}}{2^9\sqrt{3}}$$ of this ADC (w/o decimation)?

If the 4-bit ADC has INL at the 16-bit level, what will be the INL of the 8-bit ADC?

How many digital output codes will be present ? 256

# Over-Sampling



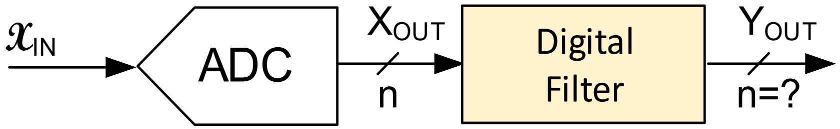
In the previous example, the Digital Filter was a MA filter, other Digital Filters could be used

Is over-sampling followed by digital filtering a practical way to increase the effective resolution of an ADC?

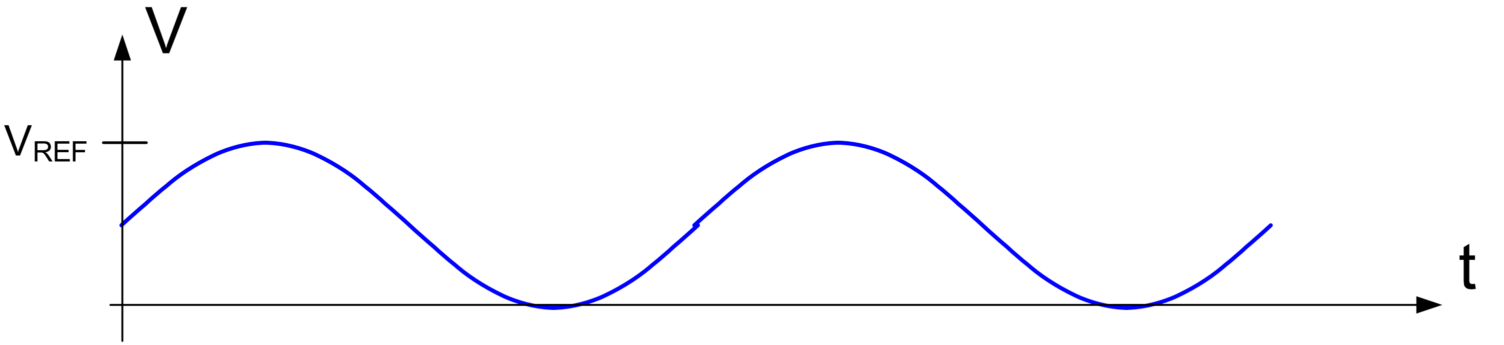
Is the digital computation overhead acceptable?

One limitation of this approach is that to get a major increase in effective resolution, the over sampling ratio gets very large since ENOB varies with the square root of the OSR

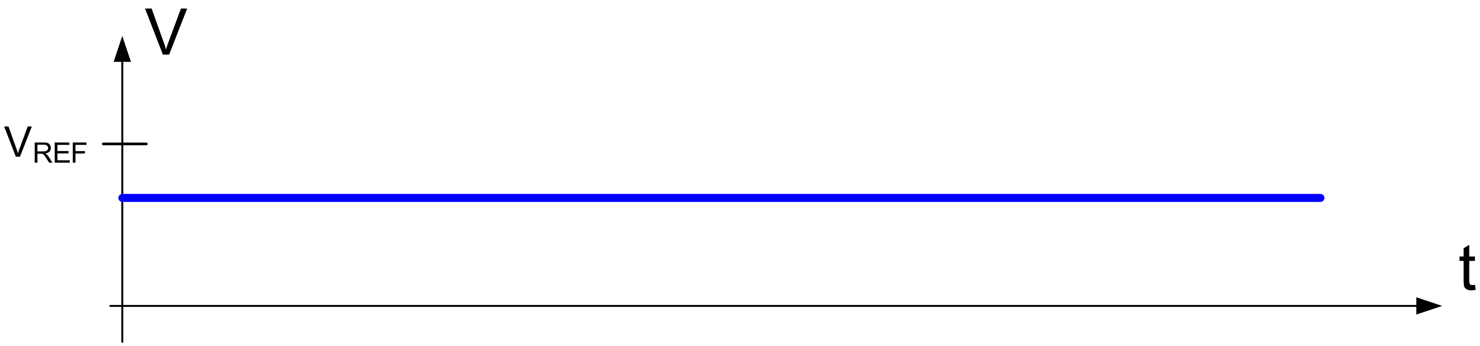
# Over-Sampling



Consider same 4-bit ADC with 16-point Moving Average digital filter



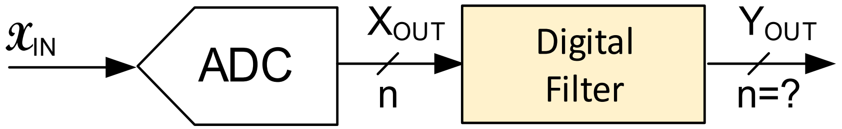
What will be the output if a constant input is applied ?



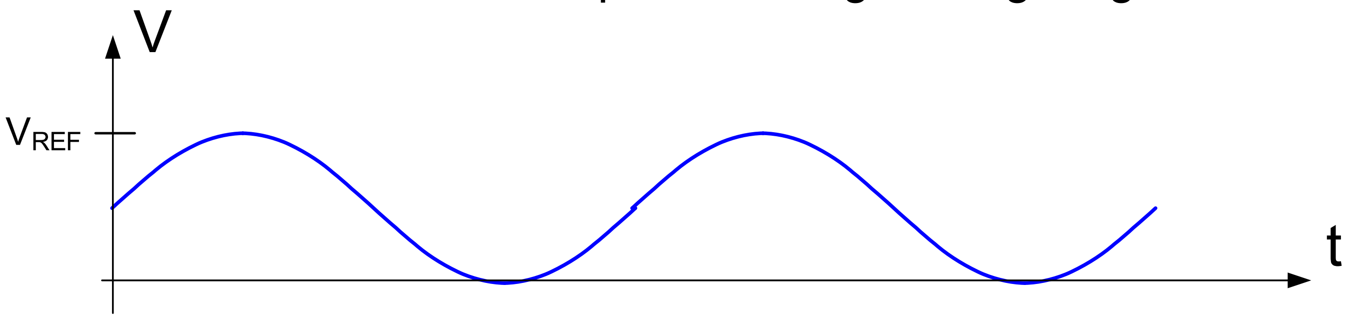
Will it still be an 8-bit output?

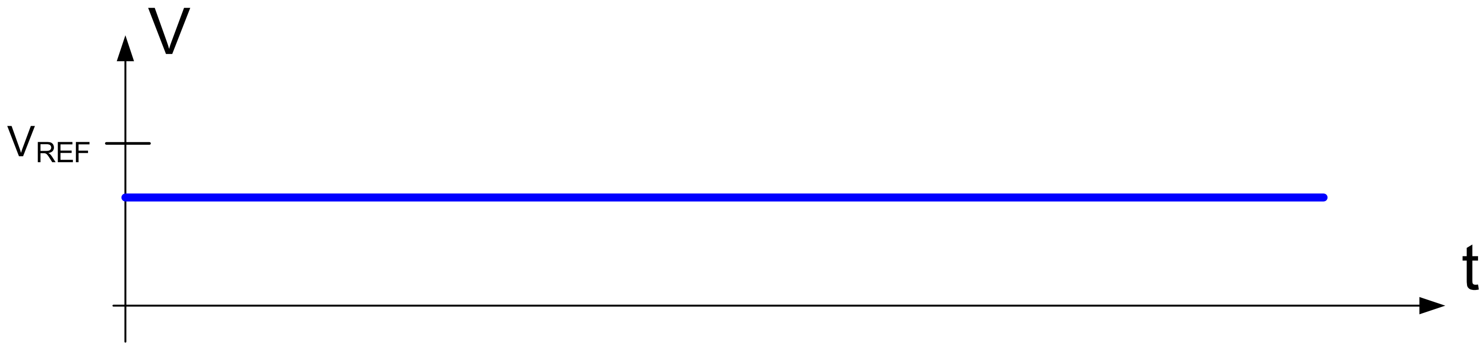
If a large number of constant input signals are applied, how many output codes will there be? 16

# Over-Sampling



Consider same 4-bit ADC with 16-point Moving Average digital filter



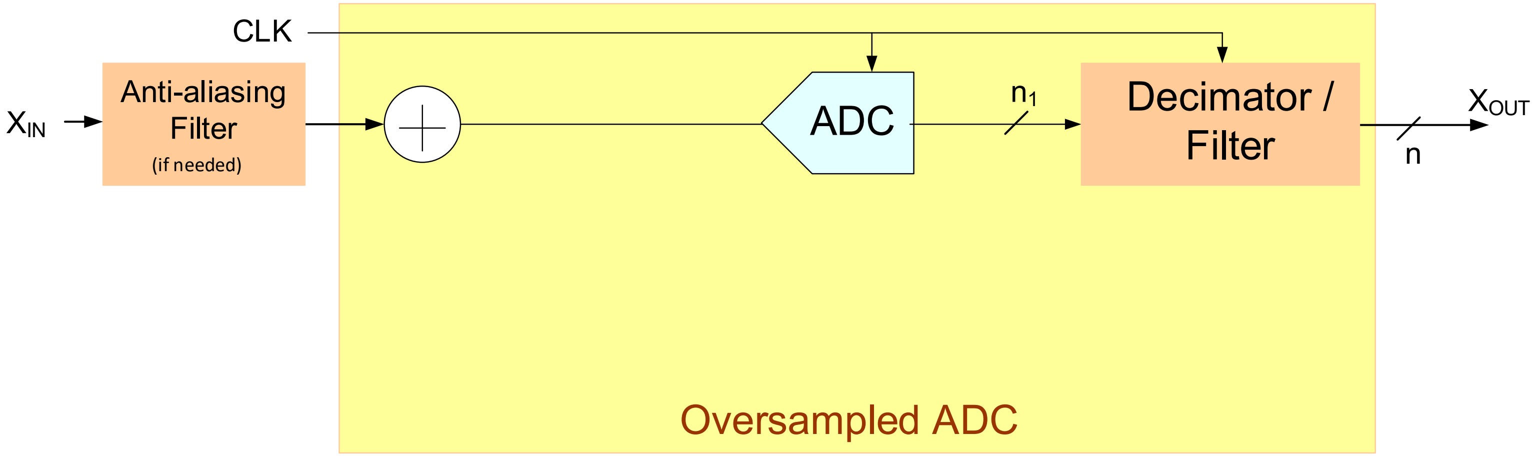


Be careful about performance relative to speckmanship !

Is there some way to actually take advantage of the over-sampling to increase the apparent resolution without facing the static resolution problem?

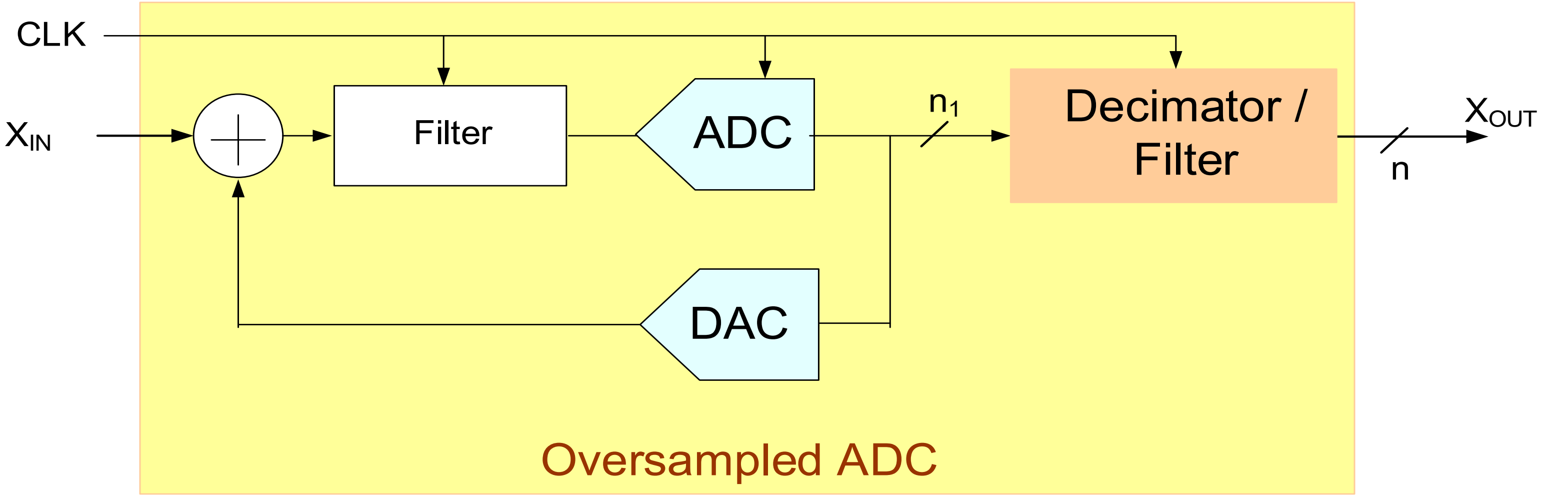
Can add random noise, or dither, or use ΔΣ modulation or other ways as well

# Over-sampled ADC



- Anti-aliasing filter at the input (if needed) to limit bandwidth of input signal
- ADC is often simply a comparator
- CLK is much higher in frequency than effective sampling rate (maybe 128:1 though lower OSR also widely used)
- Can obtain very high resolution but effective sampling rate is small
- **With clever design, this approach can reduce quantization effects and improve linearity**

# Over-sampled ΔΣ ADC (Delta-Sigma)



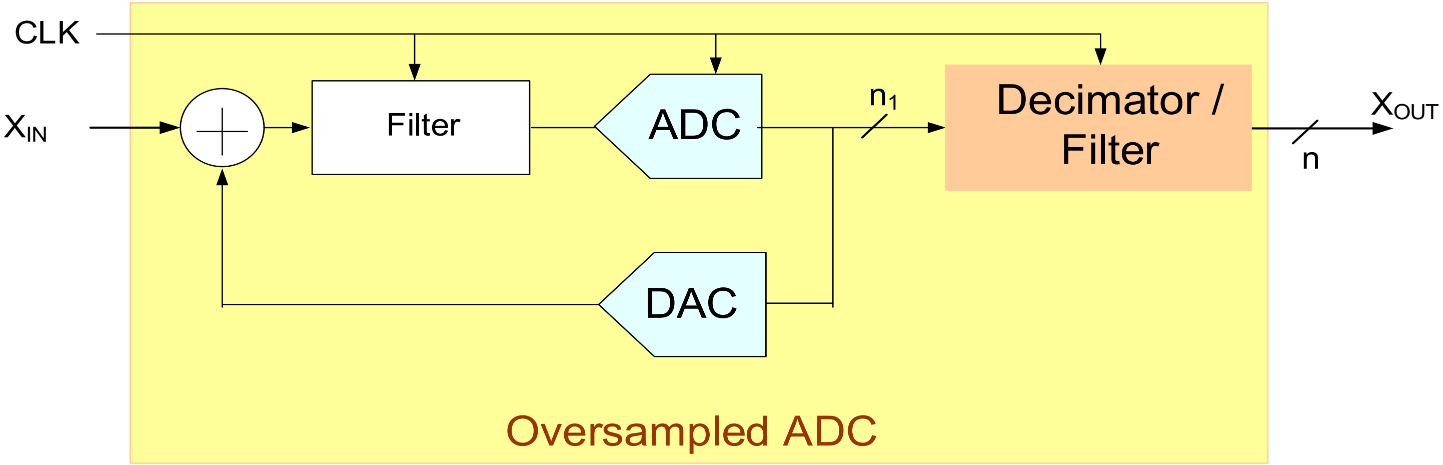
If Modulator is added, the over-sampled ADC becomes a ΔΣ ADC

Δ modulation introduced by Deloraine in 1946

ΔΣ ADC concept introduced by Yasuhiko Yasuda in the early 1960's while he was a student at the University of Tokyo

Candy (1974) and Temes credited with incorporating the concept in integrated data converters

# Over-sampled ΔΣ ADC (Delta-Sigma)

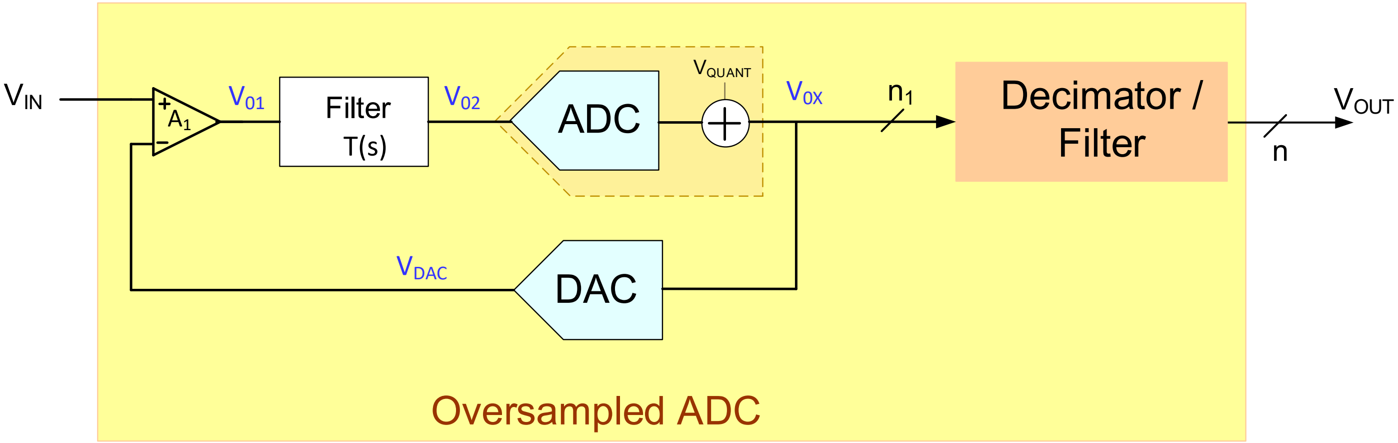


- Linearity performance almost entirely determined by that of the DAC
- 1-bit DAC (i.e. only a comparator for ADC) is inherently linear and widely used
- 20-bit linearity is achievable without any trimming using 1-bit DAC

Example: To obtain 16-bit linearity with a 10-bit DAC, the 10-bit DAC must be linear to at least the 16-bit level. This would usually require tedious trimming of the DAC

# Analysis of Delta-Sigma ADC

(big benefit is noise shaping)



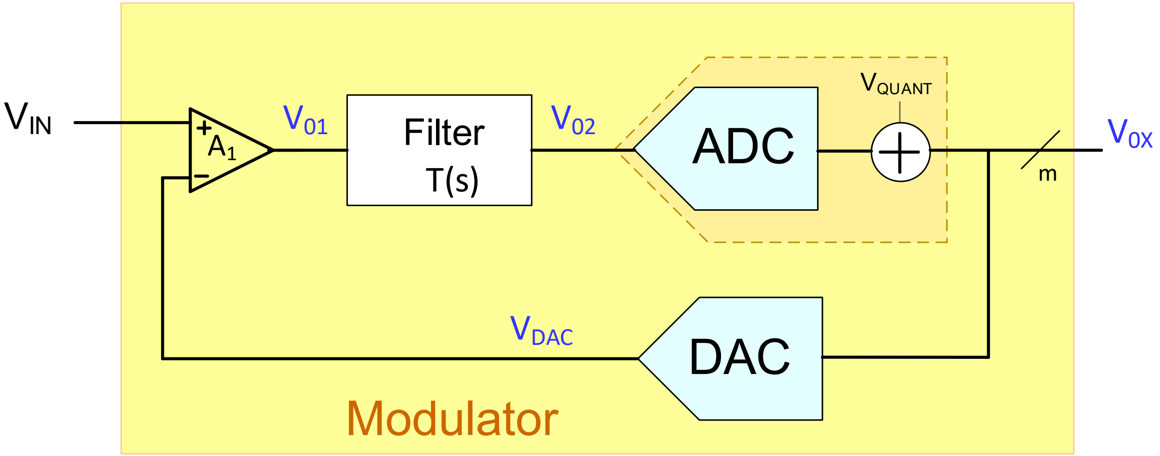
Assume ADC and DAC have unity gain (for convenience only)

Model the ADC as an ideal ADC with a quantization noise source

Decimator/Filter follow the modulator so can be neglected in analysis of modulator

# Analysis of Delta-Sigma ADC

(big benefit is noise shaping)



$$V_{01} = A_1\left(V_{IN} - V_{DAC}\right)$$

$$V_{02} = T\left(s\right)V_{01}$$

$$V_{OX} = V_{O2} + V_{QUANT}$$

$$V_{DAC} = V_{OX}$$

Solving, we obtain

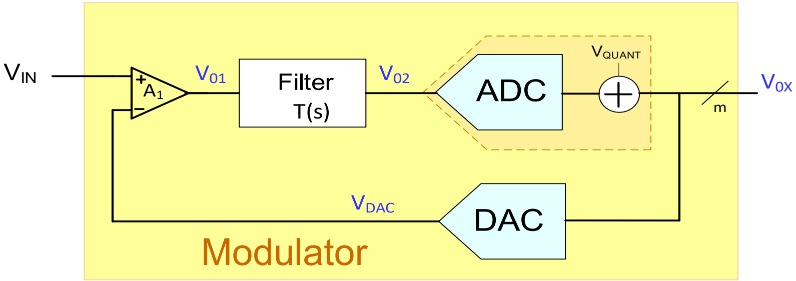
$$V_{OX} = \frac{T\left(s\right)A_1}{1+T\left(s\right)A_1}V_{IN} + V_{QUANT}\frac{1}{1+T\left(s\right)A_1}$$

Note: Significantly different transfer functions for $V_{IN}$ and $V_{QUANT}$

# Analysis of Delta-Sigma ADC

(big benefit is noise shaping)

$$V_{OX} = \frac{T(s)A_1}{1+T(s)A_1} V_{IN} + V_{QUANT} \frac{1}{1+T(s)A_1}$$



Consider using an integrator for T(s)

$$T(s) = \frac{I_{01}}{s}$$

$I_{01}$ is the unity gain frequency of the integrator and is a critical parameter in the modulator

Thus

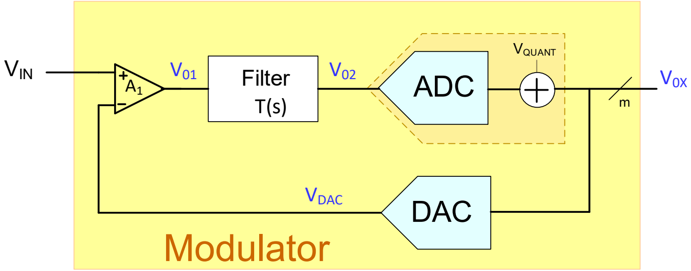
$$V_{OX} = \frac{I_{01}A_1}{s+I_{01}A_1} V_{IN} + V_{QUANT} \frac{s}{s+I_{01}A_1}$$

Note $V_{IN}$ is low-pass filtered and $V_{QUANT}$ is high-pass filtered and both are first-order with the same poles

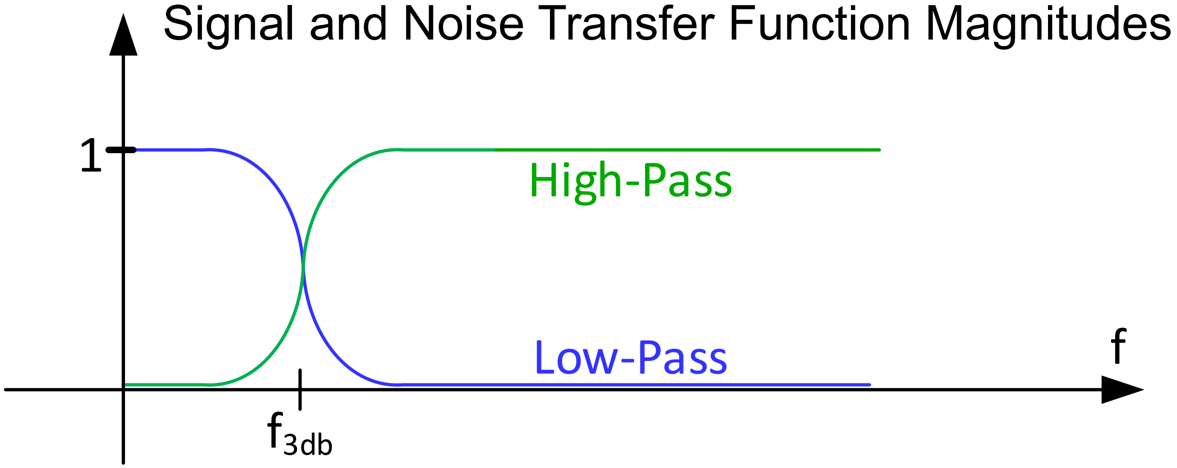
# Analysis of Delta-Sigma ADC

(big benefit is noise shaping)

$$V_{OX} = \frac{I_{01}A_1}{s + I_{01}A_1} V_{IN} + V_{QUANT} \frac{s}{s + I_{01}A_1}$$



With integrator for T(s)

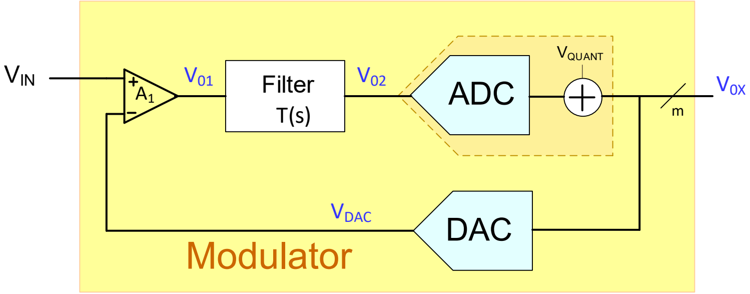


- Noise filtering will remove most of the noise from the signal band if the pole placed around signal band edge
- Signal band will not be significantly affected
- Filtering the noise is termed “noise shaping” in the vernacular of the delta-sigma community
- Since gain is 1 at high frequencies, HP filter does not increase spectral magnitude of noise at high frequencies

# Analysis of Delta-Sigma ADC

(big benefit is noise shaping)

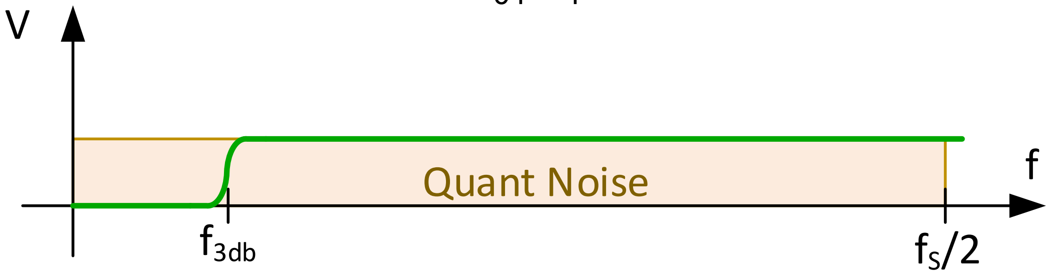
$$V_{OX} = \frac{I_{01}A_1}{s + I_{01}A_1} V_{IN} + V_{QUANT} \frac{s}{s + I_{01}A_1}$$

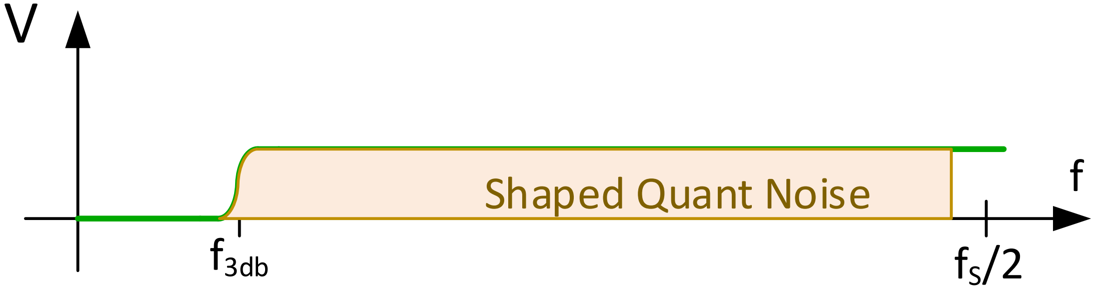


Consider the noise output first

$$V_{OX-noise} = V_{QUANT} \frac{s}{s + I_{01}A_1}$$

$$f_{3dB} = I_{01}A_1$$



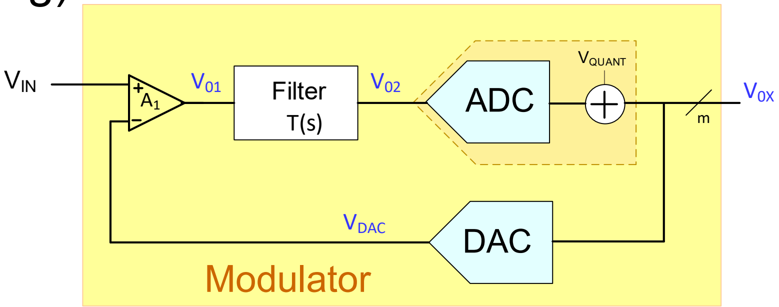


Major change in quantization noise spectral density at output

# Analysis of Delta-Sigma ADC

(big benefit is noise shaping)

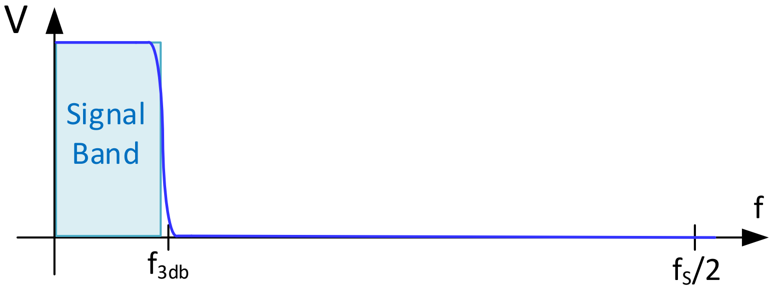
$$V_{OX} = \frac{I_{01}A_1}{s + I_{01}A_1} V_{IN} + V_{QUANT} \frac{s}{s + I_{01}A_1}$$

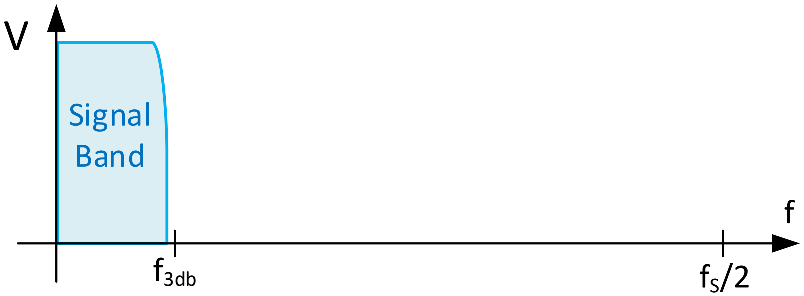


Consider the input signal

$$V_{OX-IN} = V_{IN} \frac{I_{01}A_1}{s + I_{01}A_1}$$

$$f_{3dB} = I_{01}A_1$$



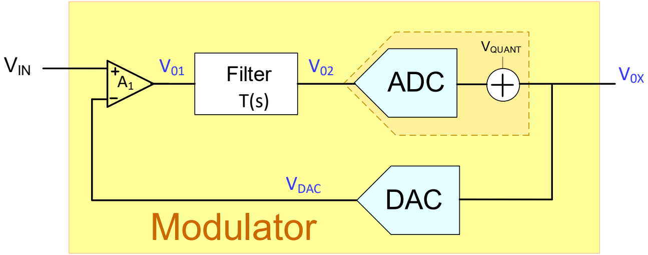


Little change in spectrum of input at the output

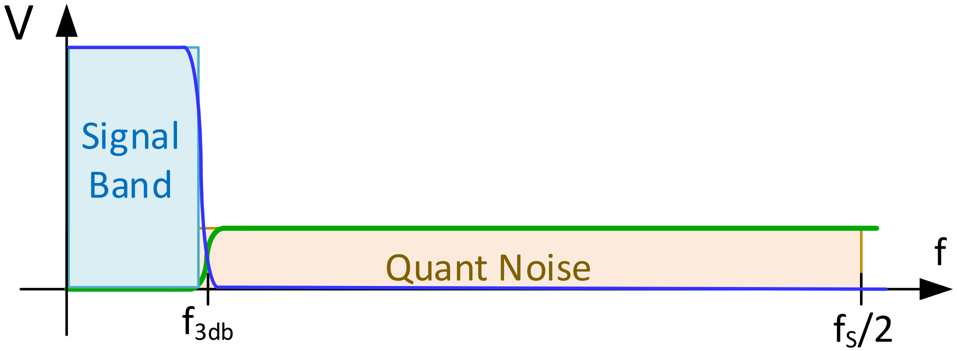
# Analysis of Delta-Sigma ADC

(big benefit is noise shaping)

$$V_{OX}=\frac{I_{01}A_1}{s+I_{01}A_1}V_{IN}+V_{QUANT}\frac{s}{s+I_{01}A_1}$$



Combined effects



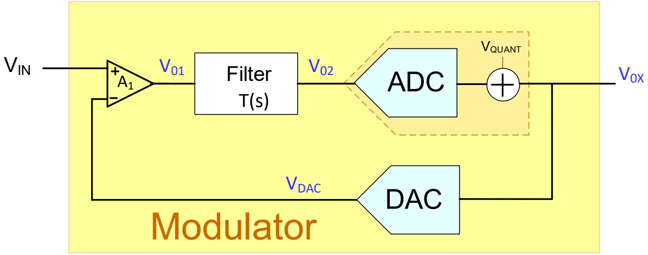
Remaining quantization noise can be dramatically reduced by a low-pass digital filter following modulator  with band-edge around $f_{3dB}$

The low-pass digital filter would have little effect on the signal band

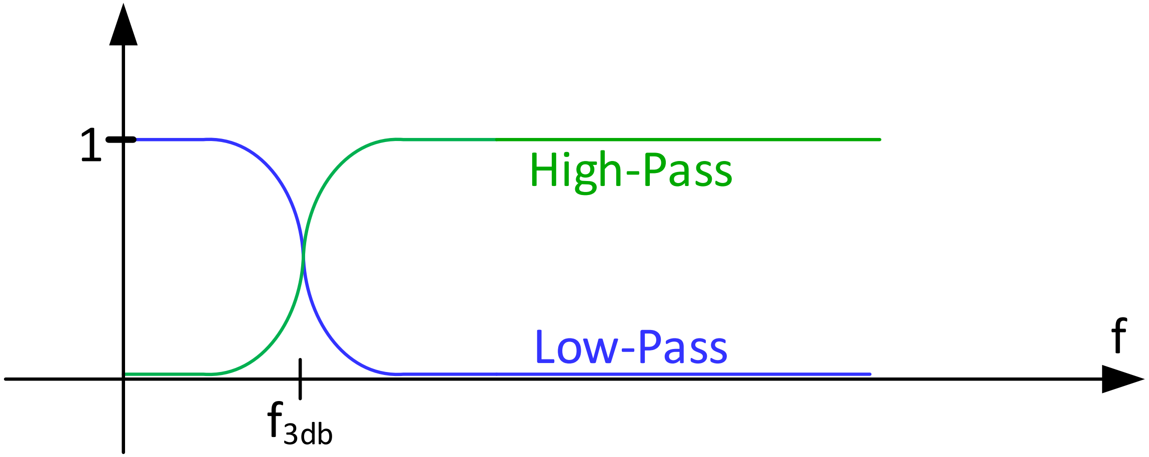
# Analysis of Delta-Sigma ADC

(big benefit is noise shaping)

$$V_{OX} = \frac{T(s)A_1}{1+T(s)A_1} V_{IN} + V_{QUANT} \frac{1}{1+T(s)A_1}$$



Signal and Noise Transfer Function Magnitudes

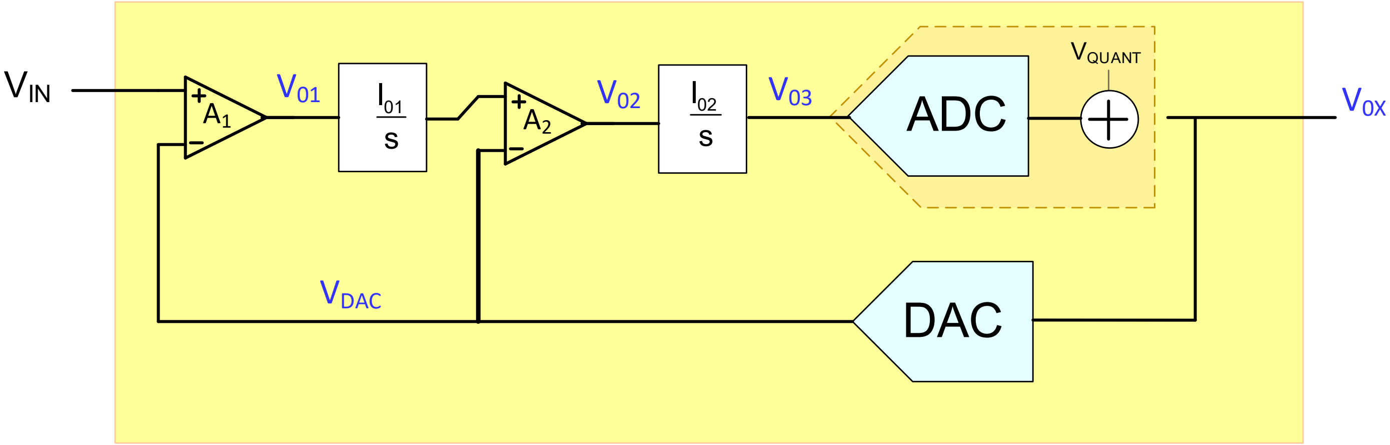


- A more selective filter (of higher order) would shape the noise even more and affect the passband even less if band edges are coincident

- Ideal low-pass and high-pass filters with coincident band edges followed by digital filter at output would allow nearly complete removal of the quantization noise !!

# Second-order Delta-Sigma ADC

(big benefit is noise shaping)



Modulator only shown with two integrators

$$V_{01} = A_1\left(V_{IN} - V_{DAC}\right)$$

$$V_{02} = A_2\left[\frac{I_{01}}{s}V_{01} - V_{DAC}\right]$$

$$V_{03} = \frac{I_{02}}{s}V_{02}$$

$$V_{OX} = V_{O3} + V_{QUANT}$$

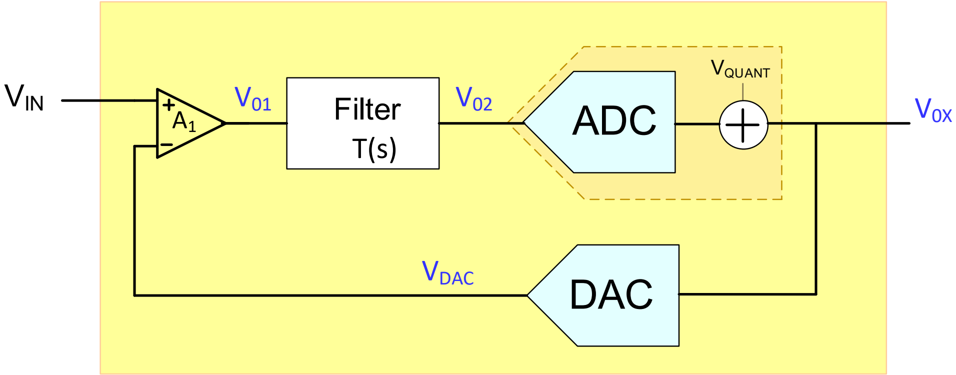
$$V_{DAC} = V_{OX}$$

Solving, obtain

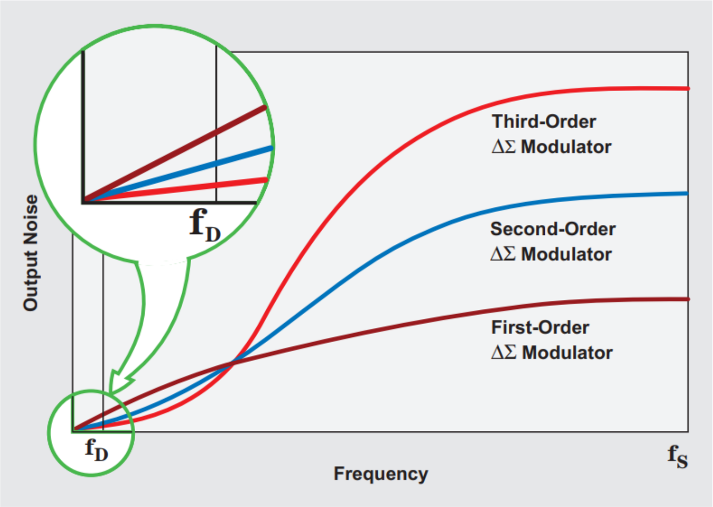
$$V_{OX} = \frac{I_{01}I_{02}A_1A_2}{s^2 + sI_{02}A_2 + I_{01}I_{02}A_1A_2}V_{IN} + \frac{s^2}{s^2 + sI_{02}A_2 + I_{01}I_{02}A_1A_2}V_{QUANT}$$

# Higher-order Delta-Sigma ADC

(big benefit is noise shaping)

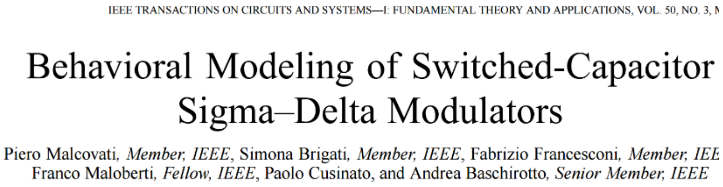


Much sharper transition between noise pass-band and signal stop band



From SLYT423 by Texas Instruments (author Bonnie Baker)

Baker reported TI used up to 6th order filters in SLYT423

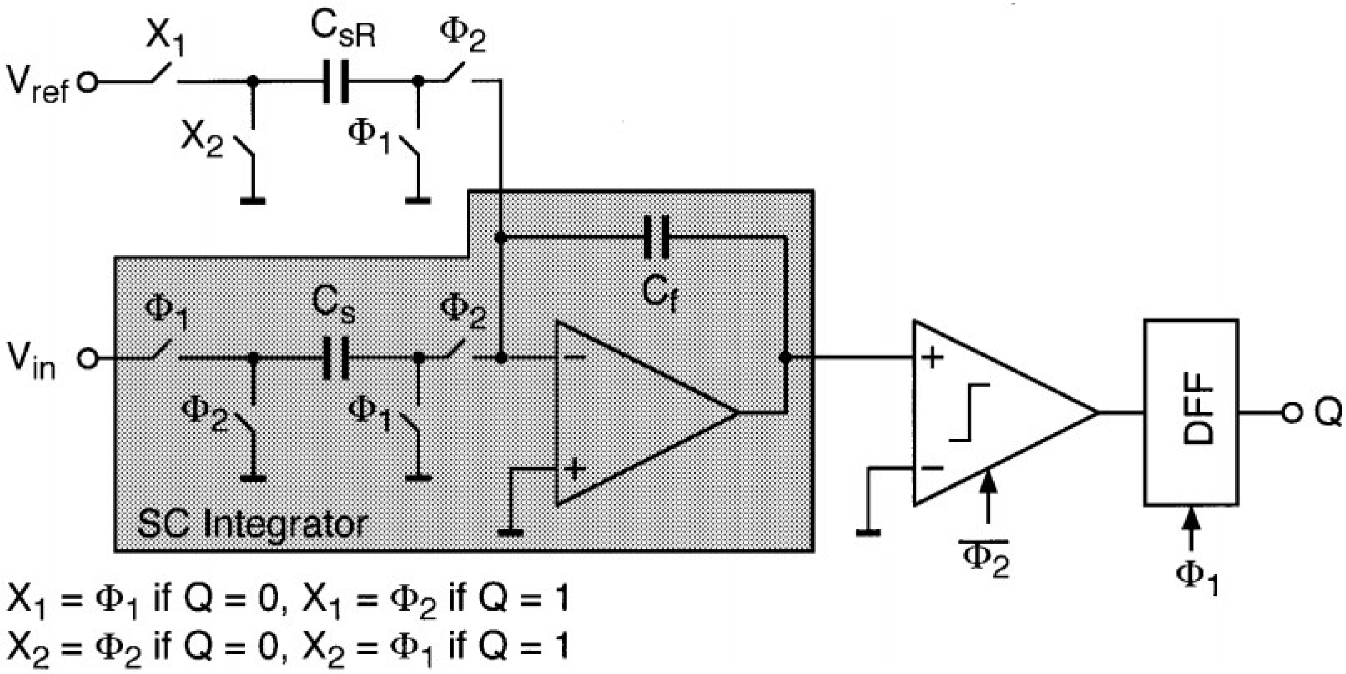


IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: FUNDAMENTAL THEORY AND APPLICATIONS, VOL. 50, NO. 3, M

Behavioral Modeling of Switched-Capacitor Sigma–Delta Modulators

Piero Malcovati, *Member, IEEE*, Simona Brigati, *Member, IEEE*, Fabrizio Francesconi, *Member, IEE*
Franco Maloberti, *Fellow, IEEE*, Paolo Cusinato, and Andrea Baschirotto, *Senior Member, IEEE*

## SC Circuits often used for Modulator



$X_1 = \Phi_1$ if $Q = 0$, $X_1 = \Phi_2$ if $Q = 1$
$X_2 = \Phi_2$ if $Q = 0$, $X_2 = \Phi_1$ if $Q = 1$

Fig. 1. Schematic of an SC first-order ΣΔ modulator.

# Over-sampled ΔΣ  ADC)

Oversampling Alone:

$$SNR = 6.02n + 1.76 + 10\log(OSR)$$

0.5 bits/octave

Oversampling  and First-Order Modulator:

$$SNR = 6.02n + 1.76 - 5.17 + 30\log(OSR)$$

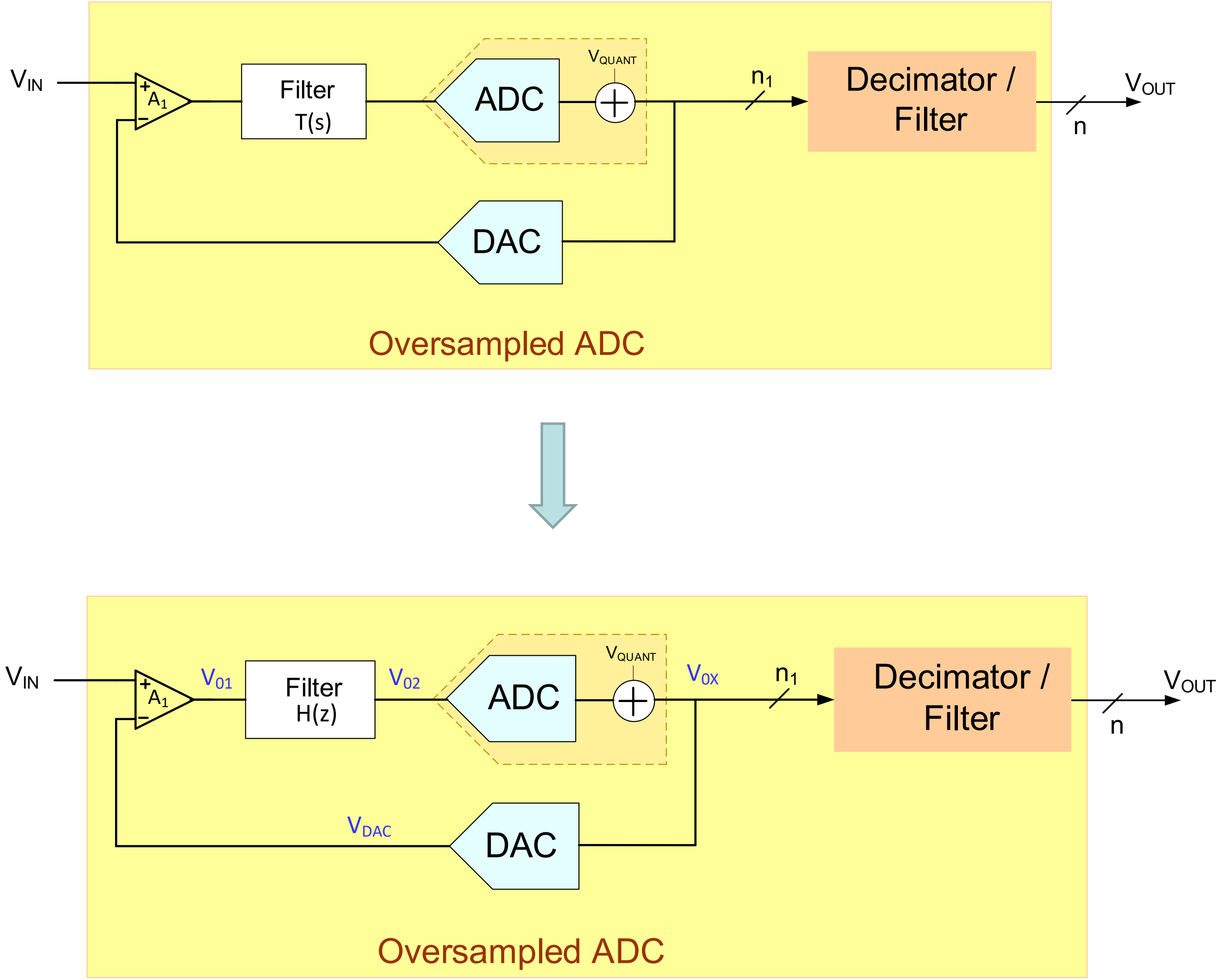
1.5 bits/octave

Oversampling  and Second-Order Modulator:

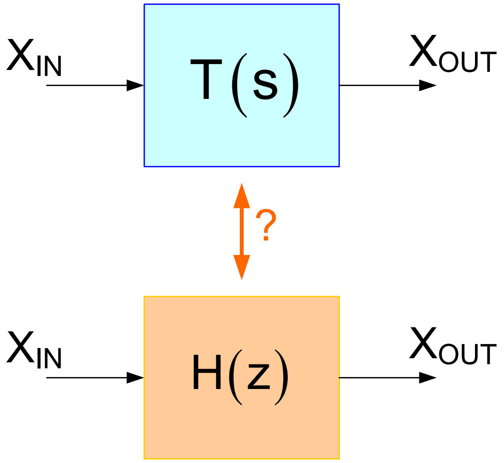
$$SNR = 6.02n + 1.76 - 12.9 + 50\log(OSR)$$

2.5 bits/octave

# Continuous-Time vs Discrete-Time  Delta-Sigma ADC



# s-domain to z-domain transformations



goal: $$T(s) = H(z)\big|_{z=e^{sT}}$$

Since can't achieve this goal, would like to map imaginary axis to unit circle and map stable filters to stable filters

consider: $$z = e^{sT}$$

$$z = e^{sT} \cong \sum_{i=0}^{\infty} \frac{1}{i!}(sT)^i$$

$$z = \sum_{i=0}^{\infty} \frac{1}{i!}(sT)^i \cong 1 + sT$$

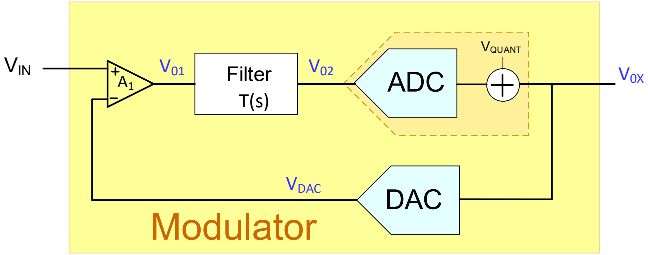
Termed the Forward Euler transformation

$$s = \frac{z-1}{T}$$

If normalized to T=1, $s = z - 1$

# Analysis of Delta-Sigma ADC

(big benefit is noise shaping)



$$V_{OX}=\frac{T(s)A_1}{1+T(s)A_1}V_{IN}+V_{QUANT}\frac{1}{1+T(s)A_1}$$

Consider using an integrator for T(s) normalized to 1 rad/sec band edge

$$T(s)=\frac{1}{s}$$ substituting $s = z -1$ $$H(z)=\frac{1}{z-1}=\frac{z^{-1}}{1-z^{-1}}$$

Thus

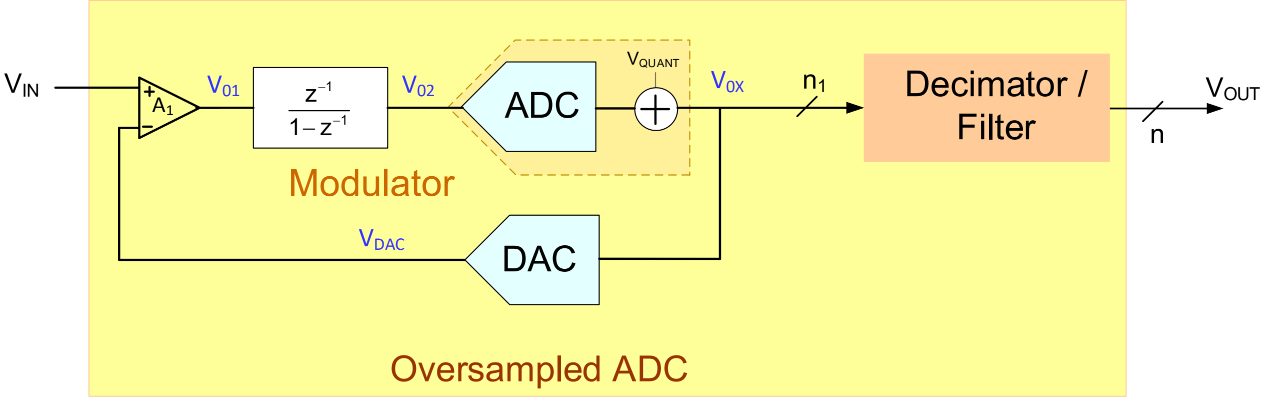
$$V_{OX}=\frac{1}{z-1+1}V_{IN}+V_{QUANT}\frac{z-1}{z-1+1}=z^{-1}V_{IN}+V_{QUANT}\left(1-z^{-1}\right)$$

Note $V_{IN}$ is low-pass filtered and $V_{QUANT}$ is high-pass filtered and both are first-order with the same poles

$STF_{NORM} = z^{-1}$ $NTF_{NORM} = 1-z^{-1}$

# Discrete-Time Delta-Sigma ADC (normalized)

(big benefit is noise shaping)



$$H(z)=\frac{1}{z-1}=\frac{z^{-1}}{1-z^{-1}}$$

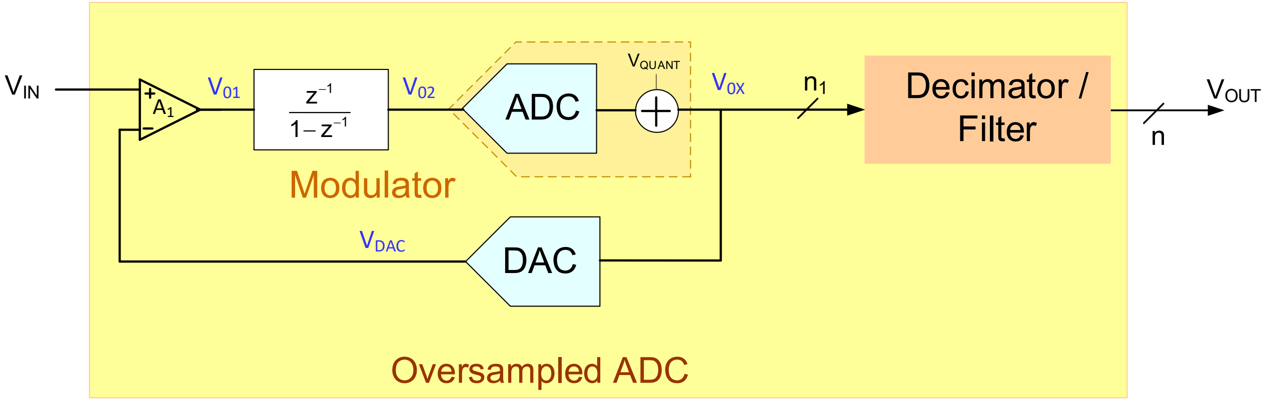
$$V_{OX}=\frac{1}{z-1+1}V_{IN}+V_{QUANT}\frac{z-1}{z-1+1}=z^{-1}V_{IN}+V_{QUANT}\left(1-z^{-1}\right)$$

Note $V_{IN}$ is low-pass filtered and $V_{QUANT}$ is high-pass filtered and both are first-order with the same poles

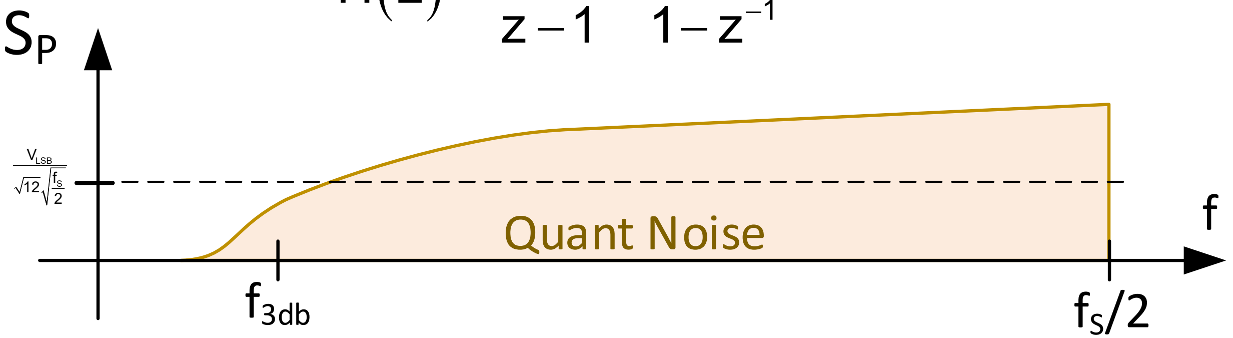
$STF_{NORM} = \ z^{-1}$ $NTF_{NORM} = \ 1-z^{-1}$

# Discrete-Time Delta-Sigma ADC (normalized)

(big benefit is noise shaping)



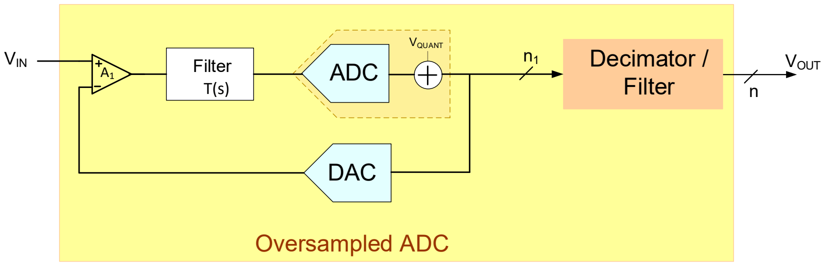
$$H(z) = \frac{1}{z-1} = \frac{z^{-1}}{1-z^{-1}}$$

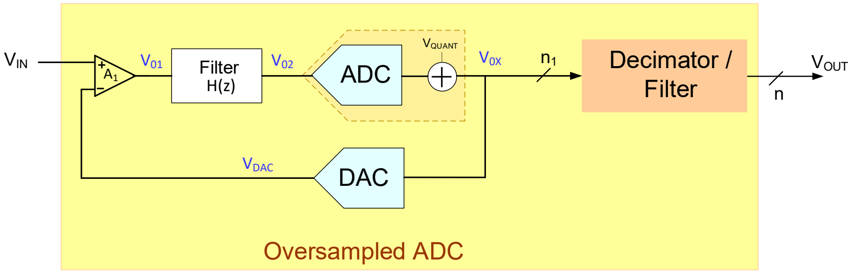


Spectral density of shaped quantization noise can be increased at higher frequencies with the high-pass noise filter

But steep cutoff in the digital filter output will still remove the high-frequency quantization noise

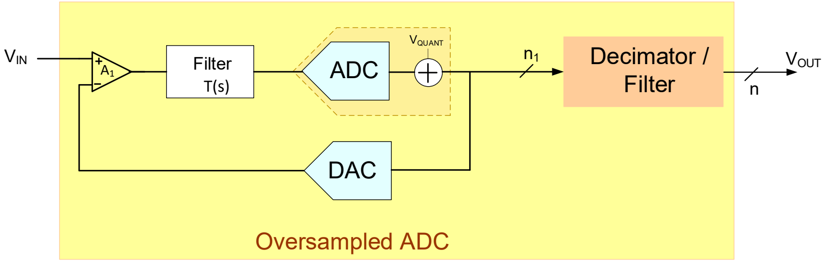
# Continuous-Time vs Discrete-Time Over-sampled Delta-Sigma ADCs

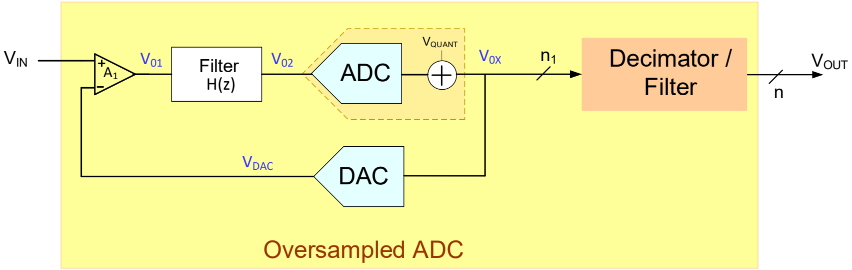




1. Input sampling errors for DT structures are never recovered
2. Nonlinearity of switches of concern in DT structures
3. No good switches in bipolar processes
4. Clock jitter adversely affects performance of discrete-time structures
5. Slew-rate requirements higher for DT structures and signal swings generally higher too
6. DT structures need additional headroom for switch control
7. CT structures can operate at lower supply voltages and lower power levels
8. Linearity of filter of increased concern in CT structures (particularly when using gm-C filters)
9. Transient response of DAC of increased concern in CT structures

# Peculiar Issues with Over-sampled Delta-Sigma ADCs

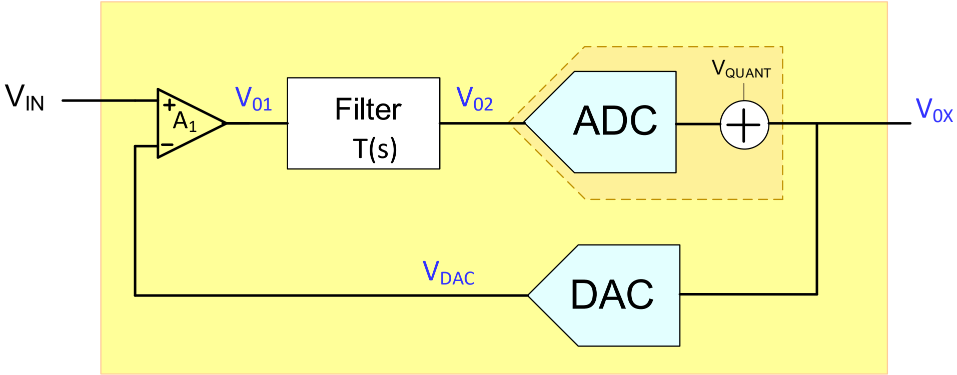




1. Increasing resolution of DAC, OSR, and filter order (in the right way) all offer potential for increasing ENOB
2. Output is not completely repeatable for a given input
3. Some dc inputs will introduce idle tones or spectral lines in the output
4. Dynamic range requirements for both the filter and the ADC may be high to avoid saturation
5. Stability analysis may be challenging and require extensive time-domain simulations (because of nonlinearities, analytically not practical)
6. OSDS-ADCs are insensitive to errors in ADC though ADC errors may increase the amount of over-range required for filter
7. Although nonlinearity in the signal-band of the filter is important, it is usually not difficult to obtain
8. Nonlinearity errors of the DAC directly introduce nonlinearity in the OSDS-ADC so excellent DAC linearity is generally required
9. Dead zones (input regions with no output) may exist

# Higher-order Delta-Sigma ADC

(big benefit is noise shaping)



Excellent Material on Delta-Sigma ADCs

"How delta-sigma ADCs work ( Part 1 and Part 2)"

Author: Bonnie Baker

SLYT423 Revised Sept 2016 by Texas Instruments

TUTORIAL 1870

# Demystifying Delta-Sigma ADCs

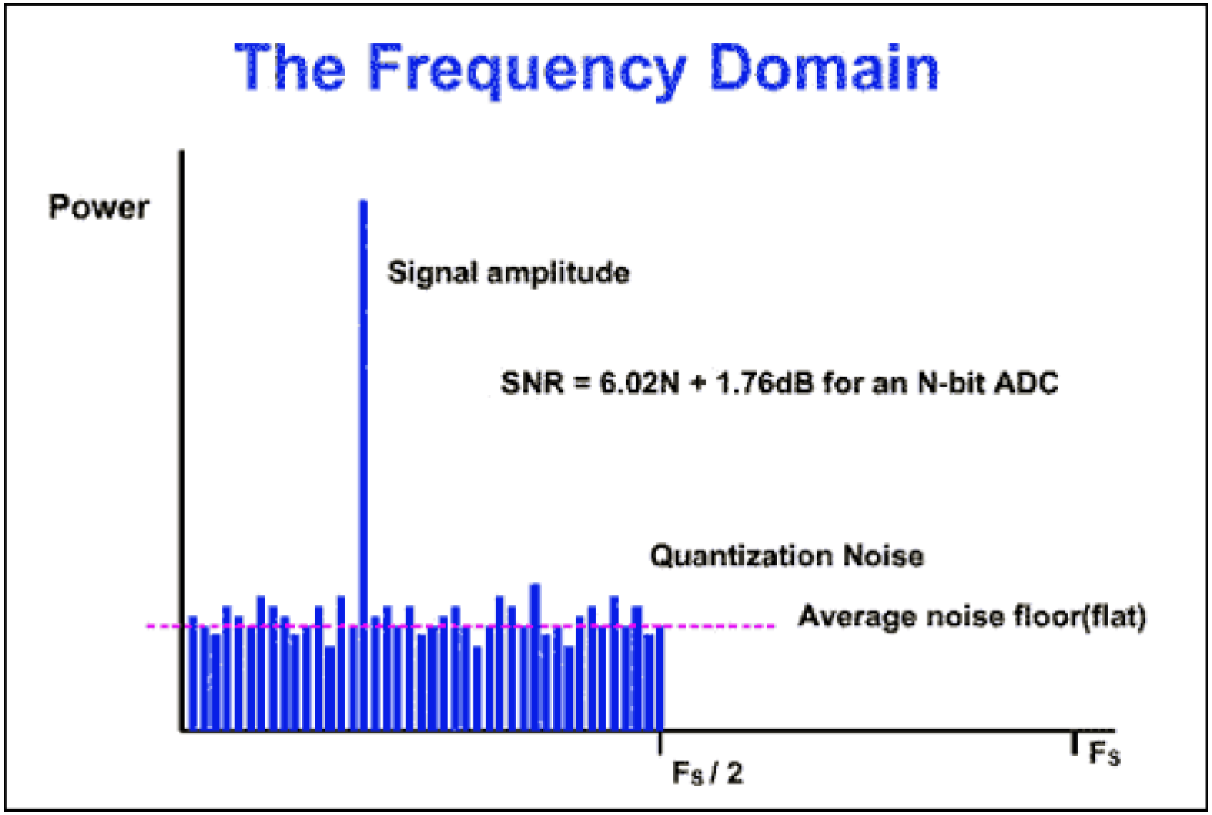


*Figure 1. FFT diagram of a multi-bit ADC with a sampling frequency $F_S$.*

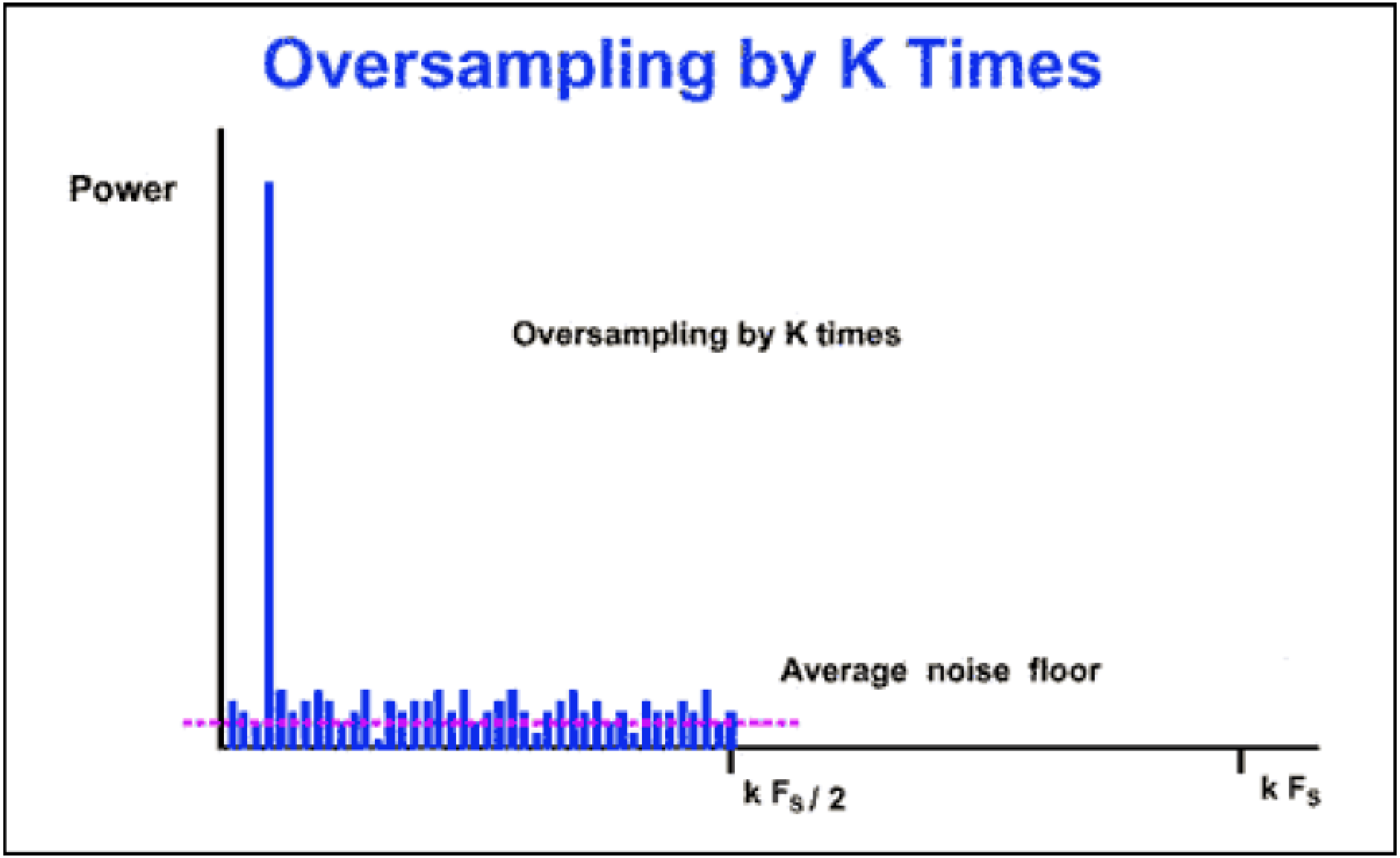


*Figure 2. FFT diagram of a multi-bit ADC with a sampling frequency $kF_S$.*

- Removal of high-frequency quantization noise
- But noise is still a problem in signal band

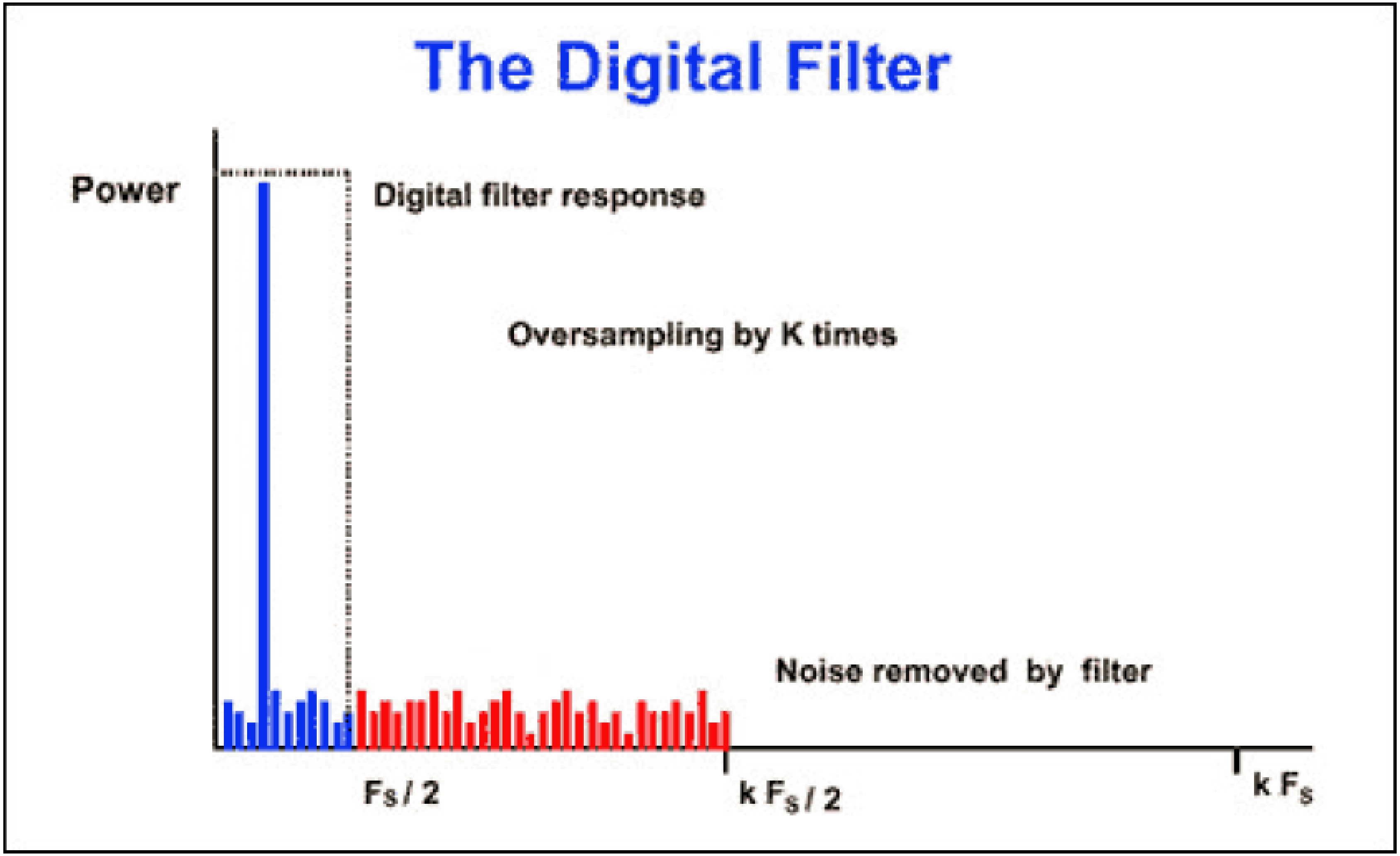


*Figure 3. Effect of the digital filter on the noise bandwidth.*

Noise reduction (noise shaping) in signal band

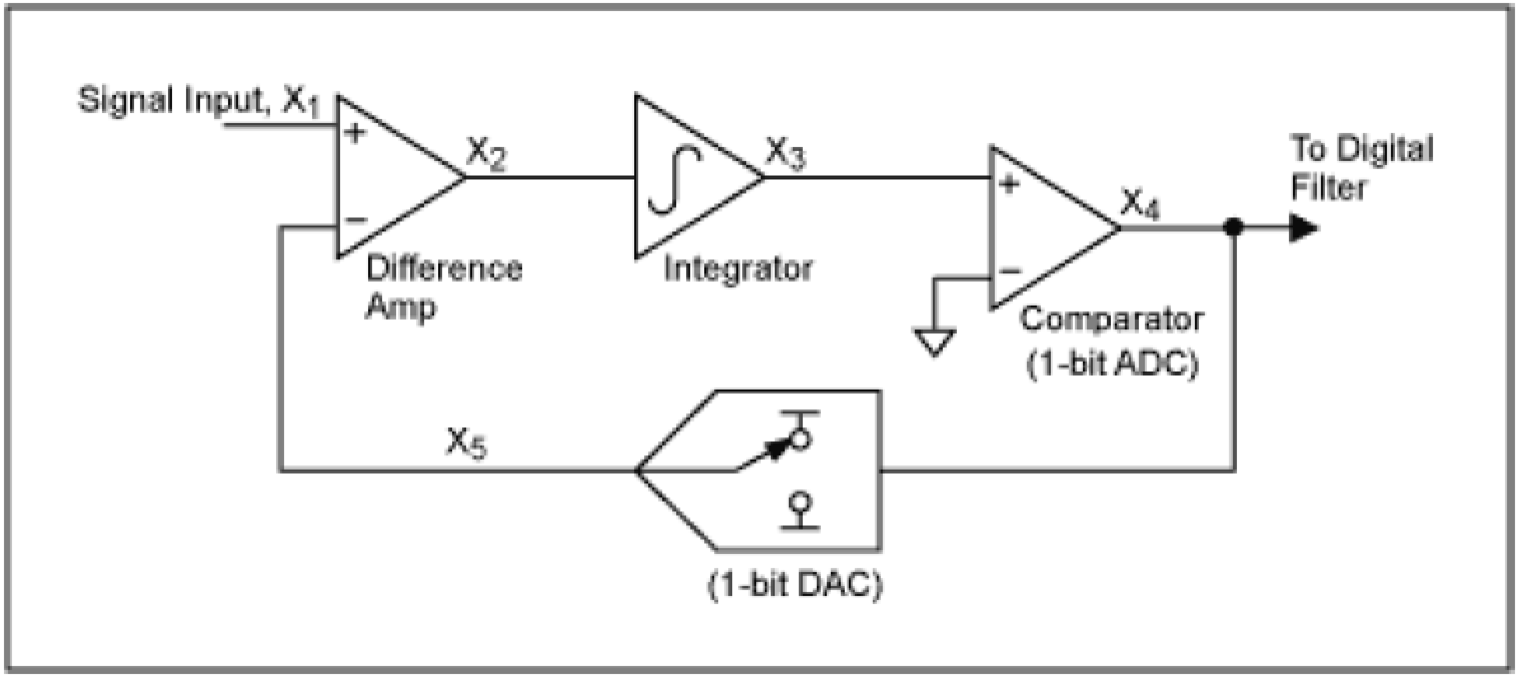


*Figure 4. Block diagram of a sigma-delta modulator.*

# Noise reduction (noise shaping) in signal band

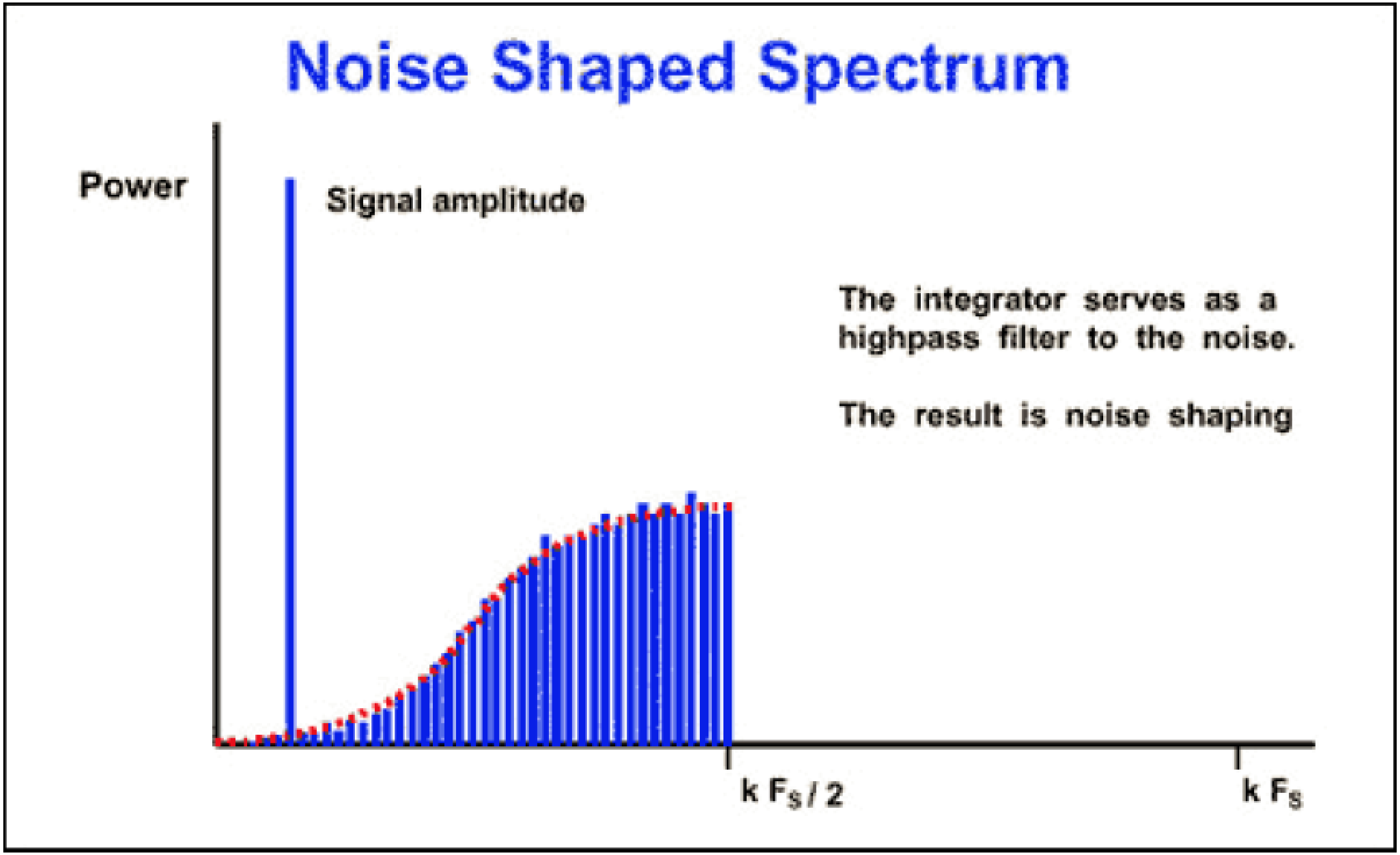


*Figure 5. Affect of the integrator in the sigma-delta modulator.*

## Noise reduction (noise shaping) in signal band

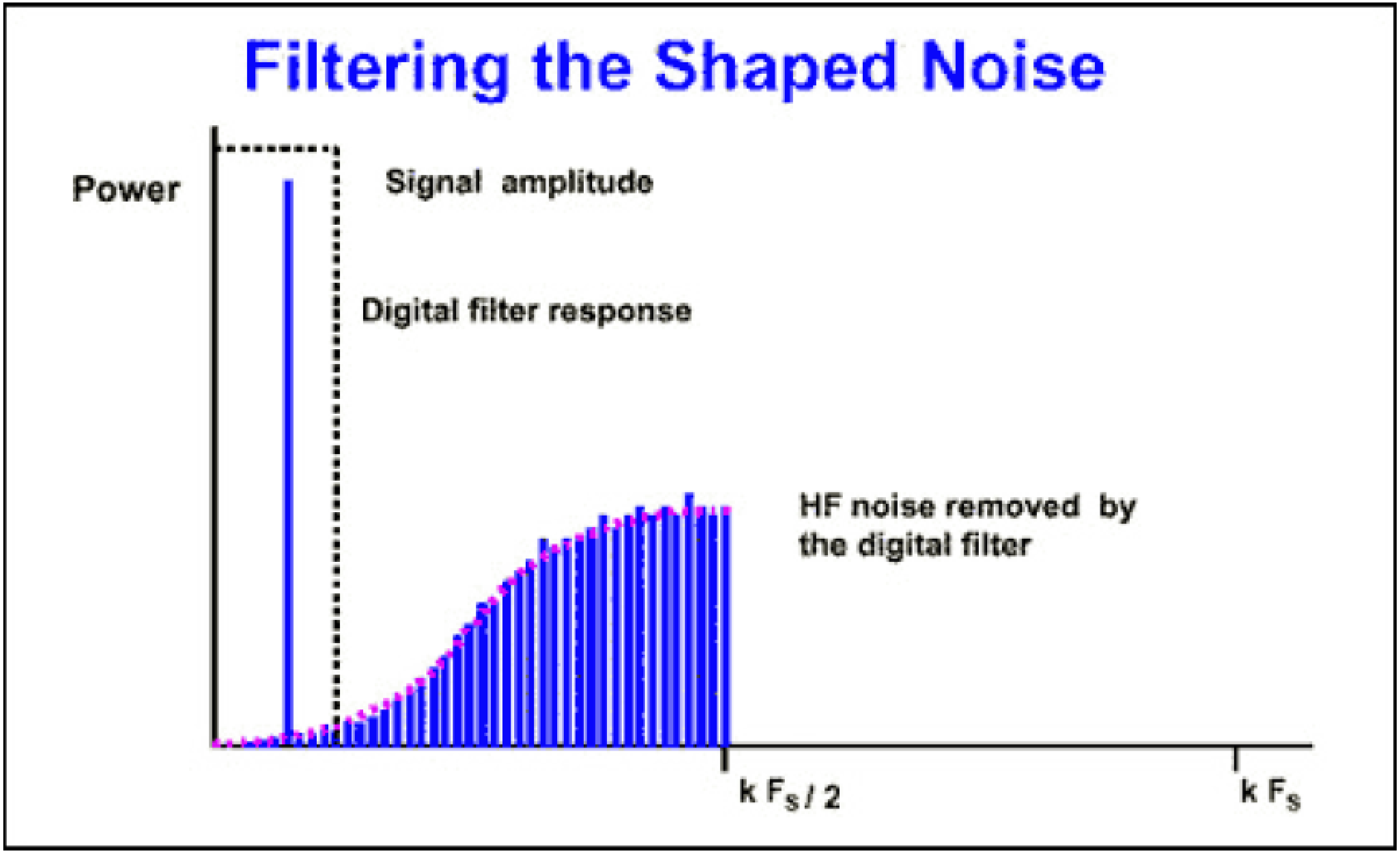


*Figure 6. Effect of the digital filter on the shaped noise.*

**AN9504**

Author: David Jarman

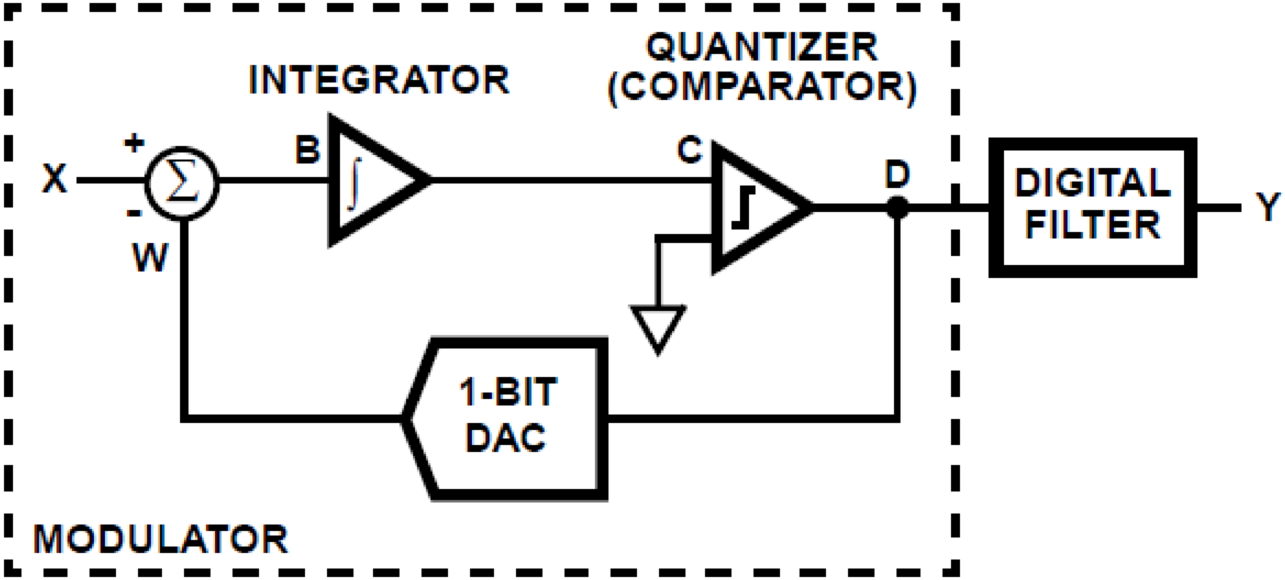
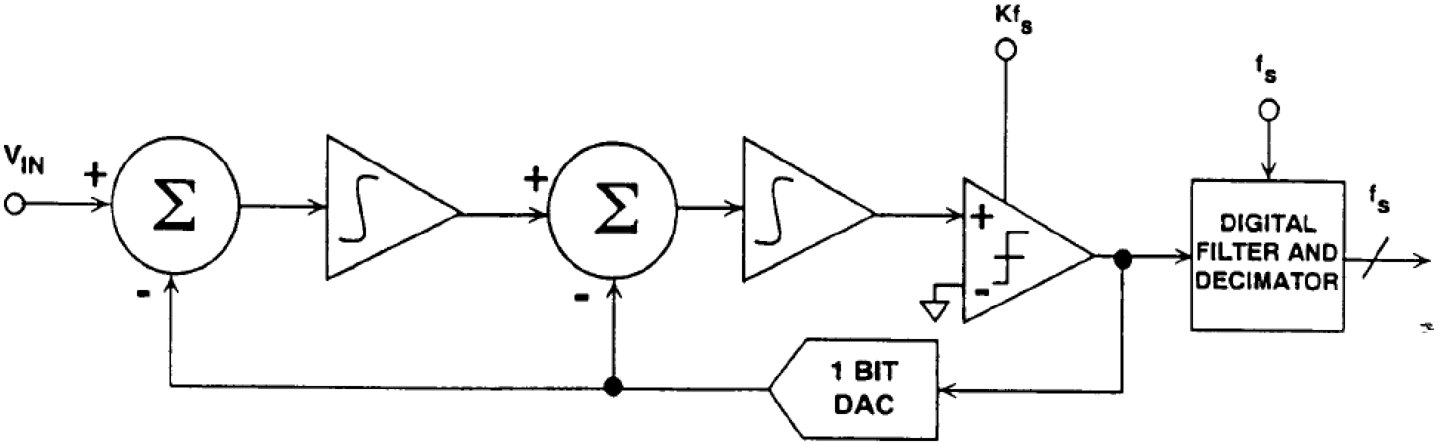


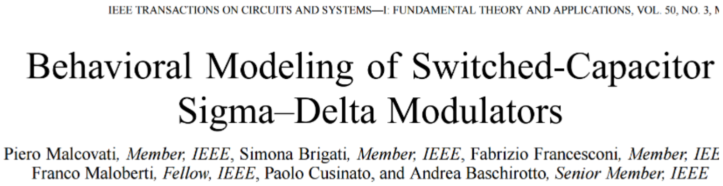
**FIGURE 1. FIRST ORDER SIGMA DELTA ADC BLOCK DIAGRAM**

ANALOG DEVICES

AN-283
APPLICATION NOTE

## SECOND-ORDER SIGMA-DELTA ADC



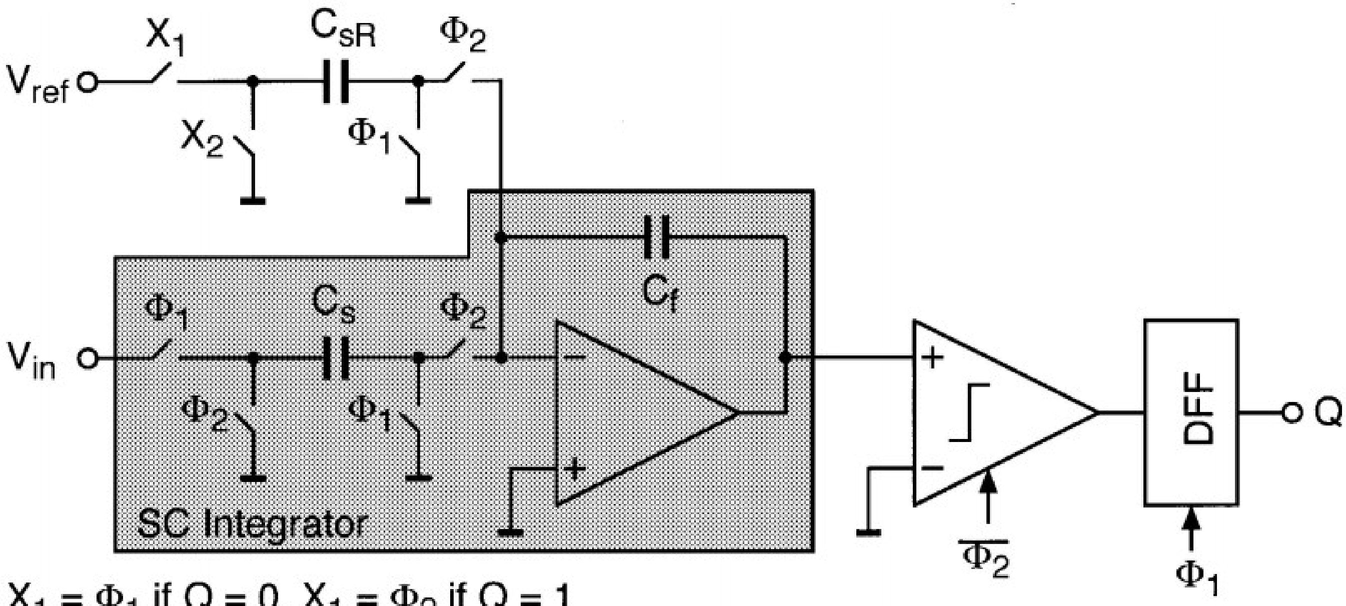


IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: FUNDAMENTAL THEORY AND APPLICATIONS, VOL. 50, NO. 3, M

Behavioral Modeling of Switched-Capacitor Sigma–Delta Modulators

Piero Malcovati, *Member, IEEE*, Simona Brigati, *Member, IEEE*, Fabrizio Francesconi, *Member, IEE*
Franco Maloberti, *Fellow, IEEE*, Paolo Cusinato, and Andrea Baschirotto, *Senior Member, IEEE*

# SC Circuits often used for Modulator



$X_1 = \Phi_1$ if $Q = 0$, $X_1 = \Phi_2$ if $Q = 1$
$X_2 = \Phi_2$ if $Q = 0$, $X_2 = \Phi_1$ if $Q = 1$

Fig. 1. Schematic of an SC first-order ΣΔ modulator.

# Over-sampled ΔΣ  ADC)

Oversampling Alone:

$$SNR = 6.02n + 1.76 + 10\log(OSR)$$

0.5 bits/octave

Oversampling  and First-Order Modulator:

$$SNR = 6.02n + 1.76 - 5.17 + 30\log(OSR)$$

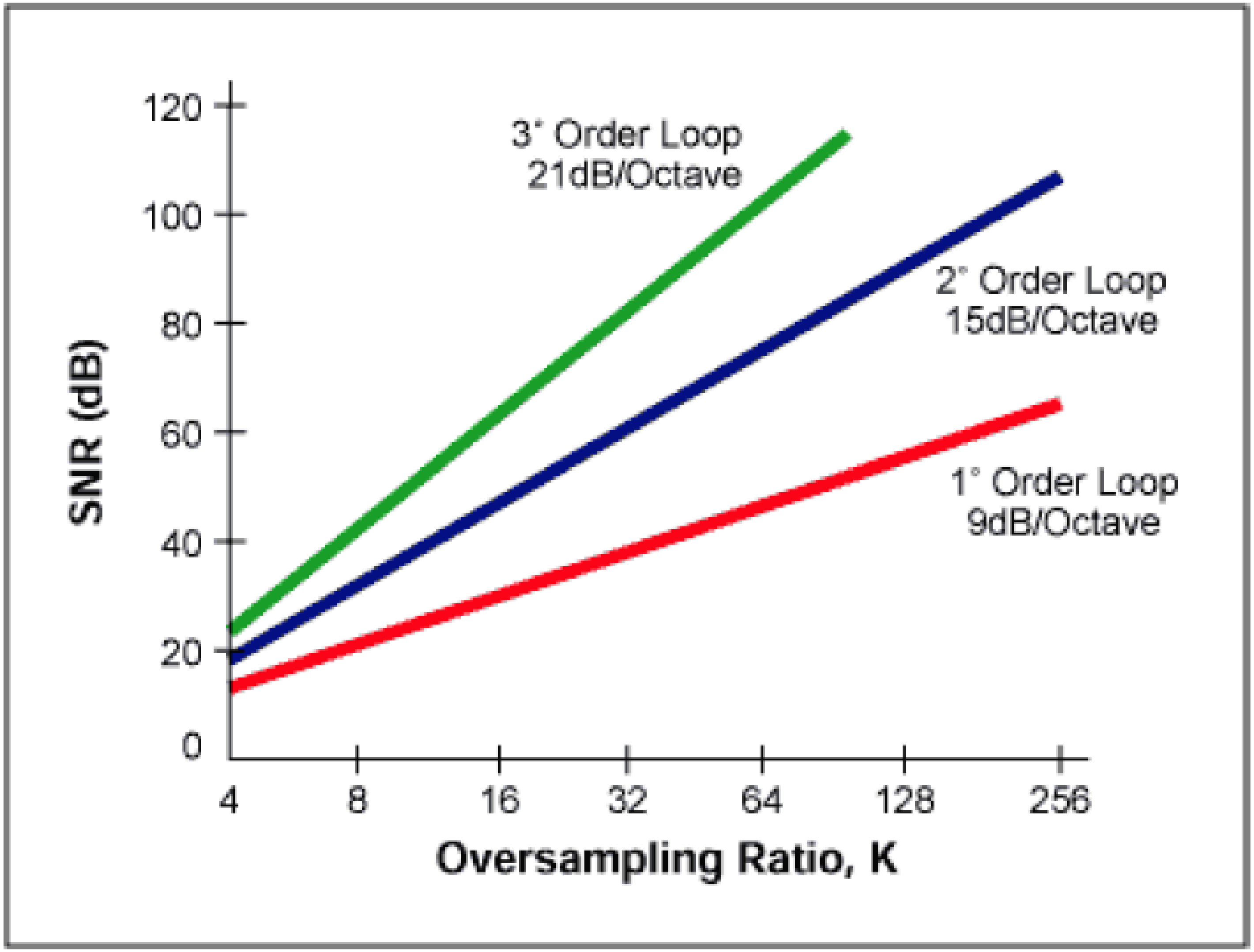
1.5 bits/octave

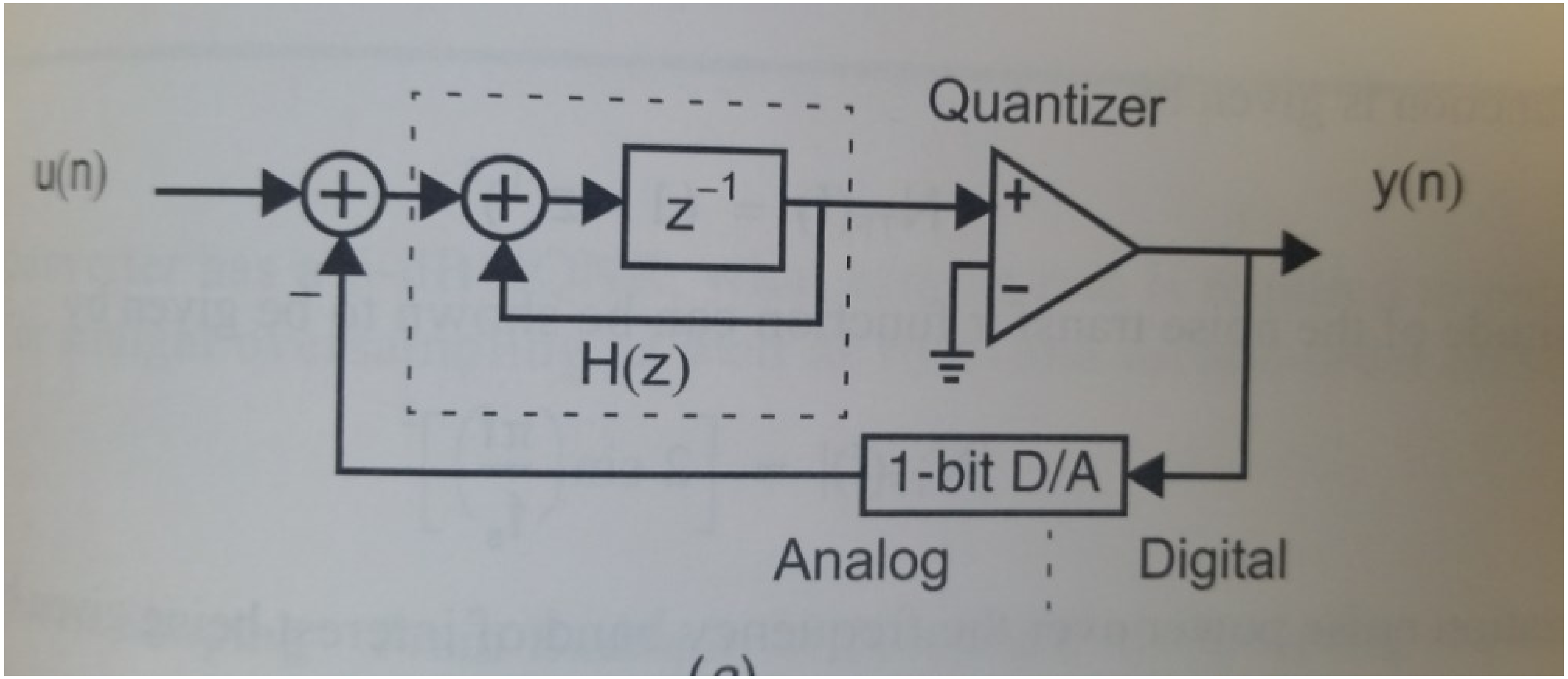
Oversampling  and Second-Order Modulator:

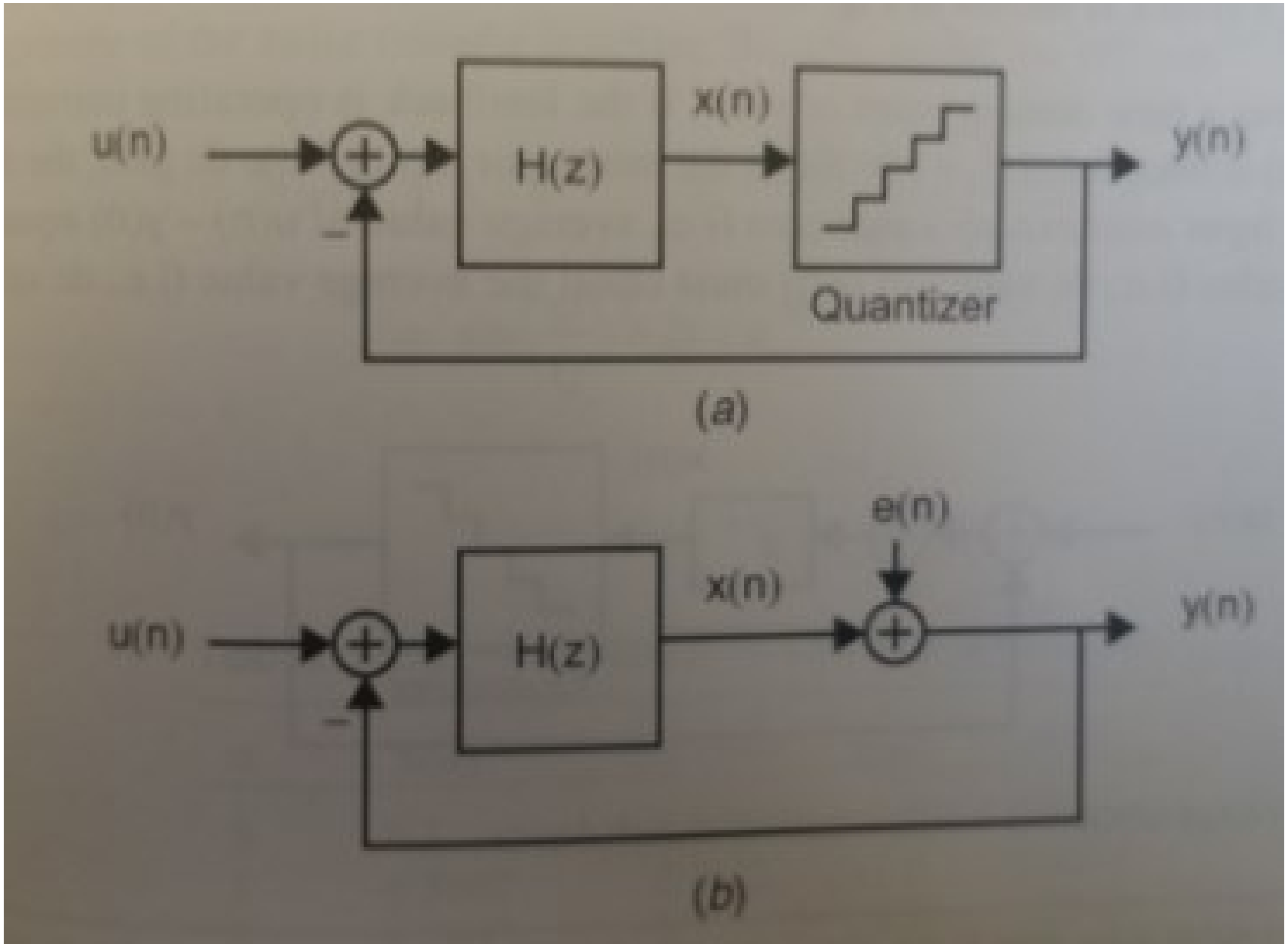
$$SNR = 6.02n + 1.76 - 12.9 + 50\log(OSR)$$

2.5 bits/octave

Noise reduction (noise shaping) in signal band

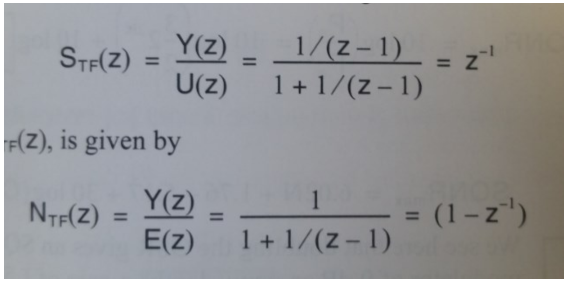



Quantizer
u(n)
y(n)
+
−
−
z^{−1}
H(z)
1-bit D/A
Analog
Digital



(a)

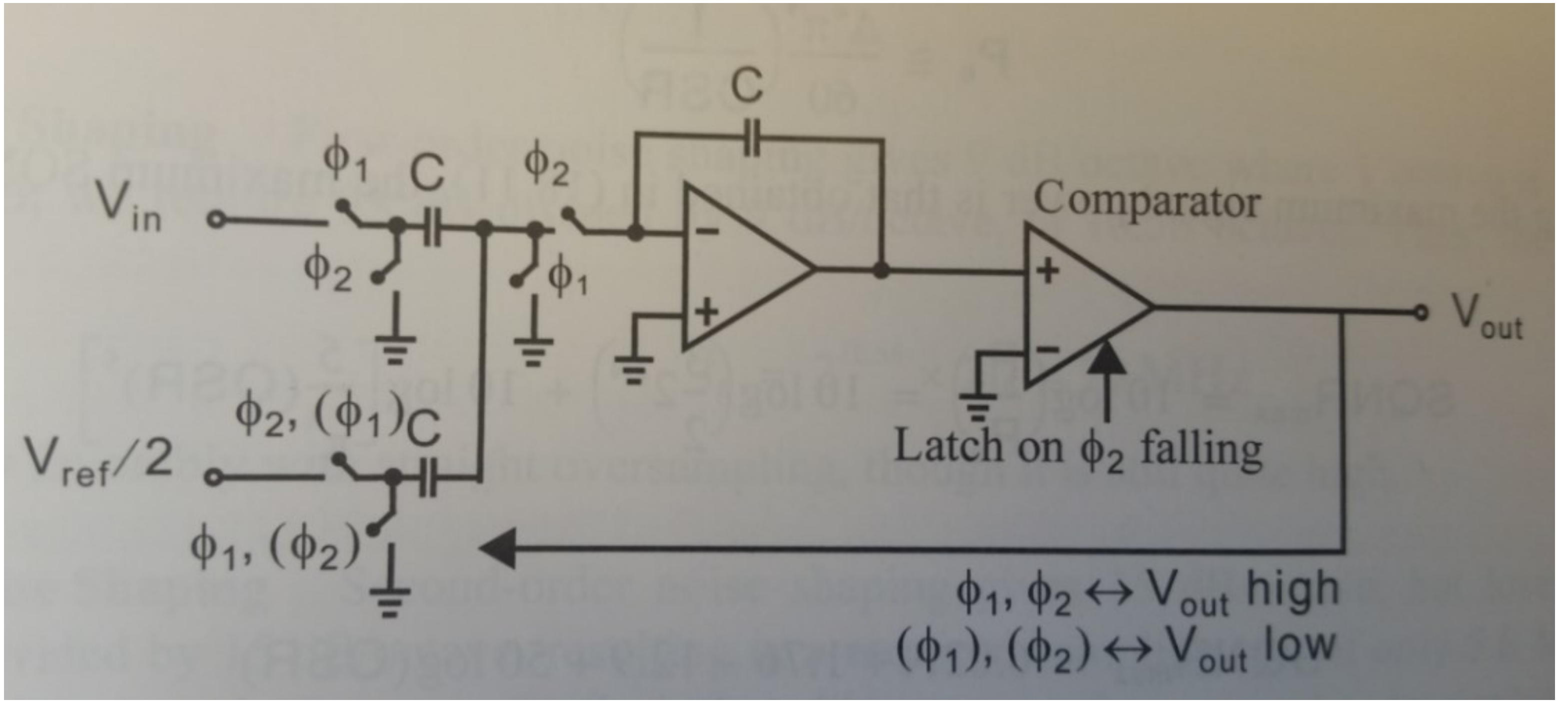
(b)

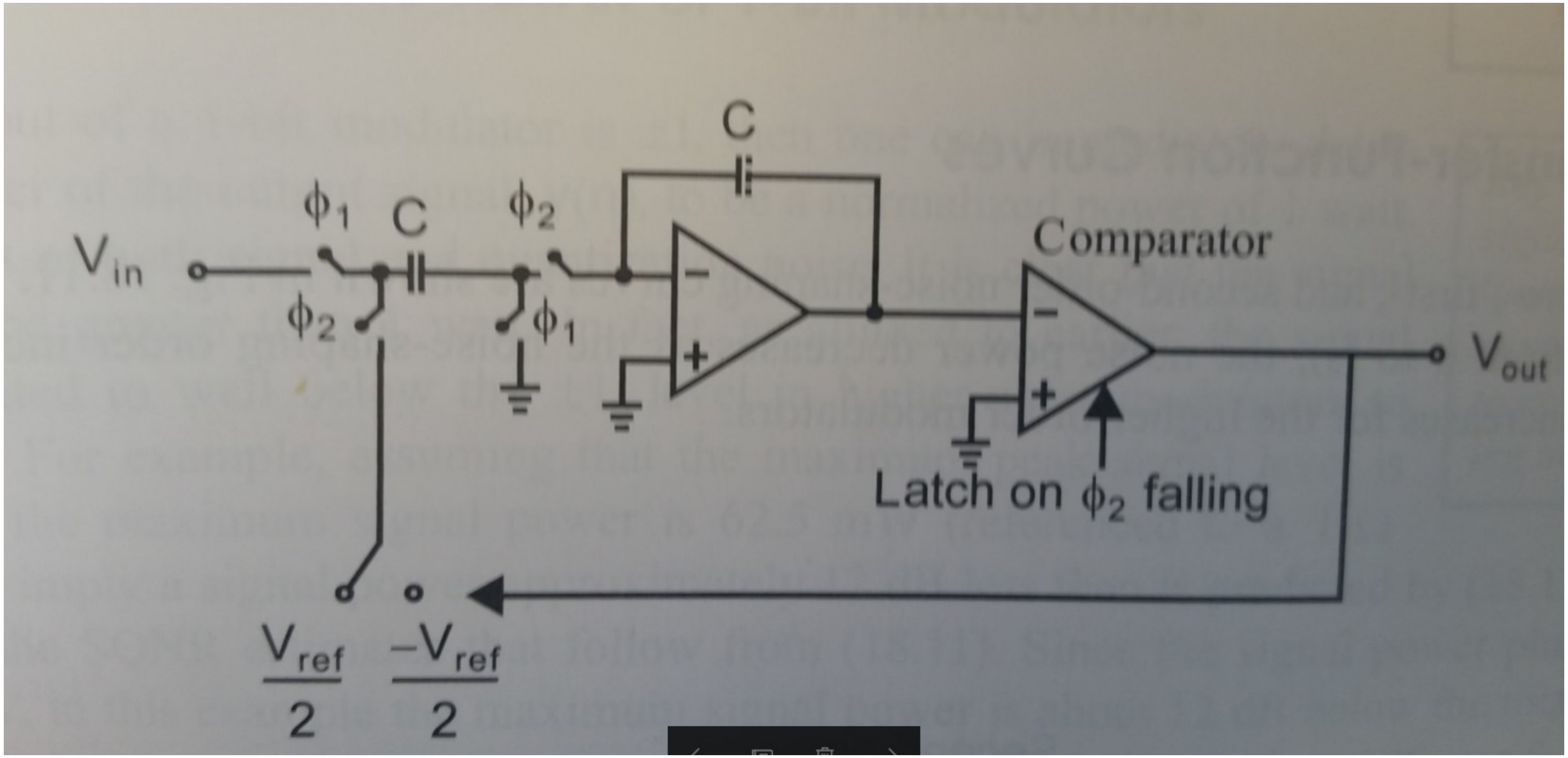


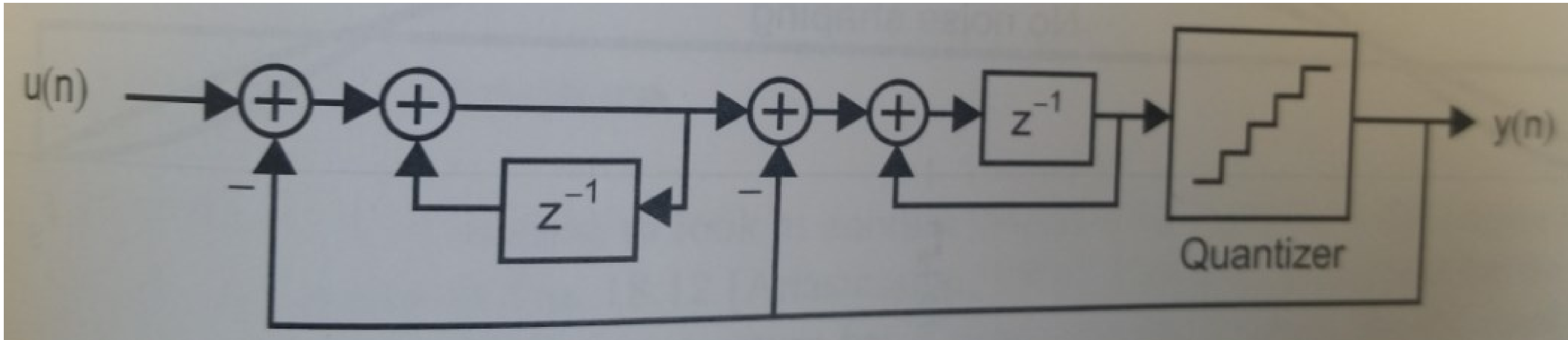
$$S_{TF}(z) = \frac{Y(z)}{U(z)} = \frac{1/(z-1)}{1+1/(z-1)} = z^{-1}$$

$_{TF}(z)$, is given by

$$N_{TF}(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+1/(z-1)} = (1-z^{-1})$$


$V_{in}$
$\phi_1$
C
$\phi_2$
$\phi_2$
$\phi_1$
C
Comparator
$V_{out}$
$\phi_2, (\phi_1)$
C
$V_{ref}/2$
$\phi_1, (\phi_2)$
Latch on $\phi_2$ falling
$\phi_1, \phi_2 \leftrightarrow V_{out}$ high
$(\phi_1), (\phi_2) \leftrightarrow V_{out}$ low


C
φ1
C
φ2
V_in
φ2
φ1
−
+
Comparator
−
+
V_out
Latch on φ2 falling
V_ref / 2
−V_ref / 2



econd-order ΔΣ modulator.

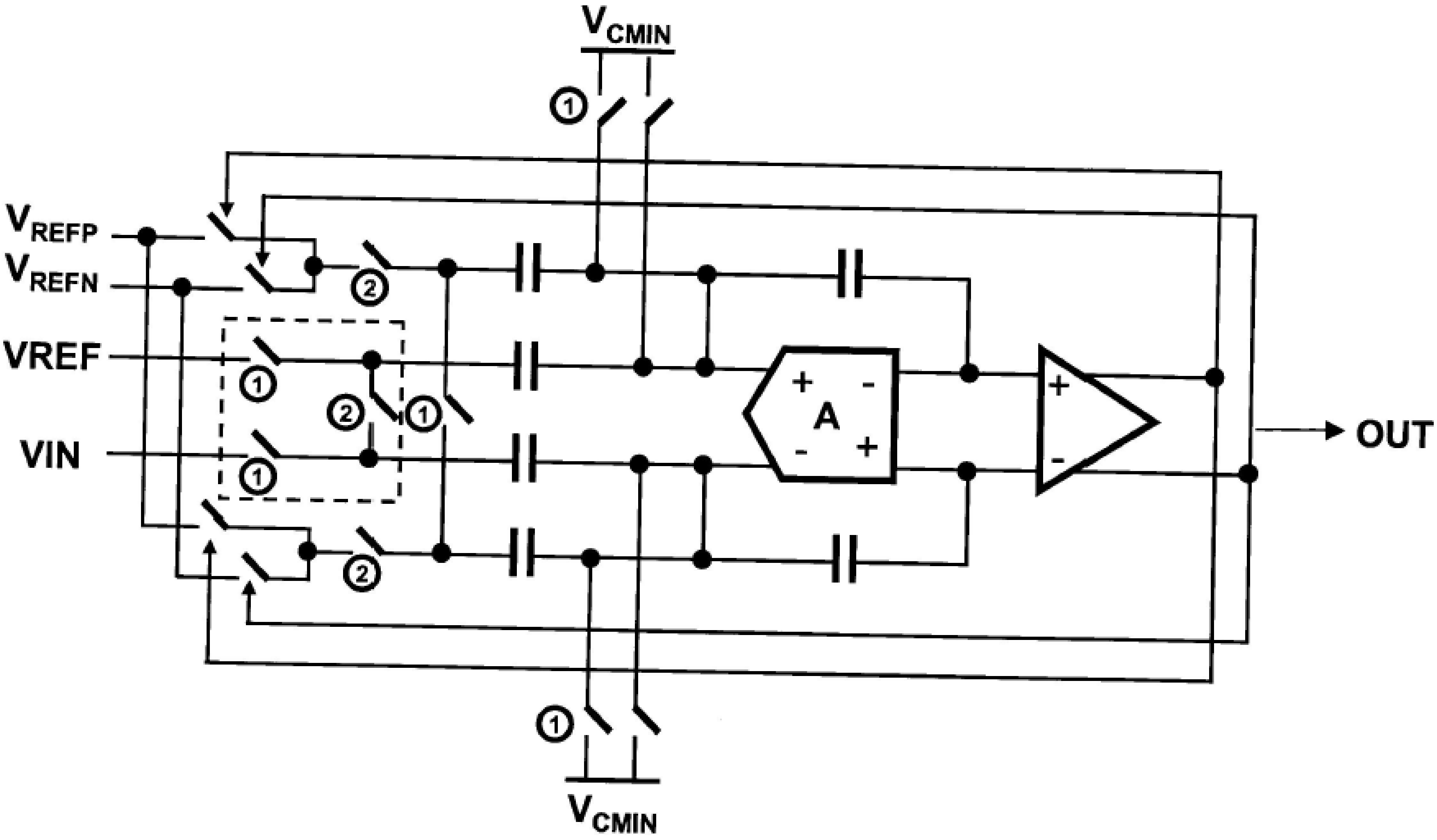


Figure 2: 1st Order Delta-Sigma ADC

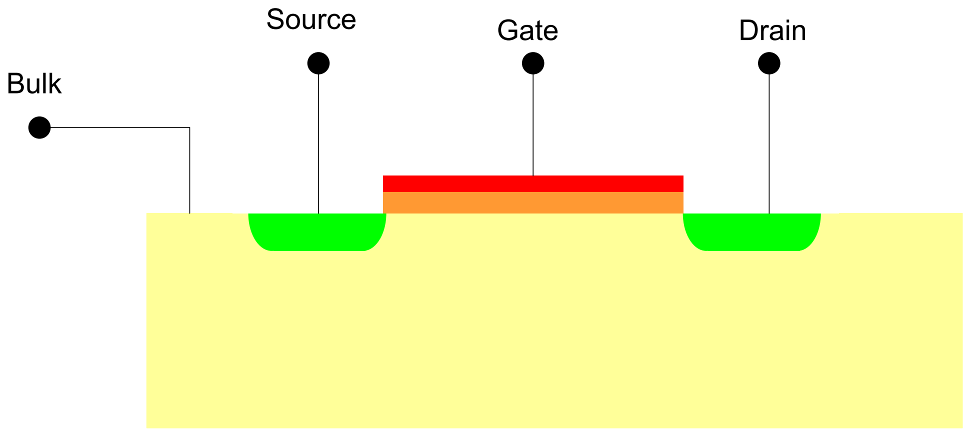
# Layout Issues for Matching Critical Components

Layout plays a critical role in determining performance of most matching-critical circuits and is of particular concern in most data converters

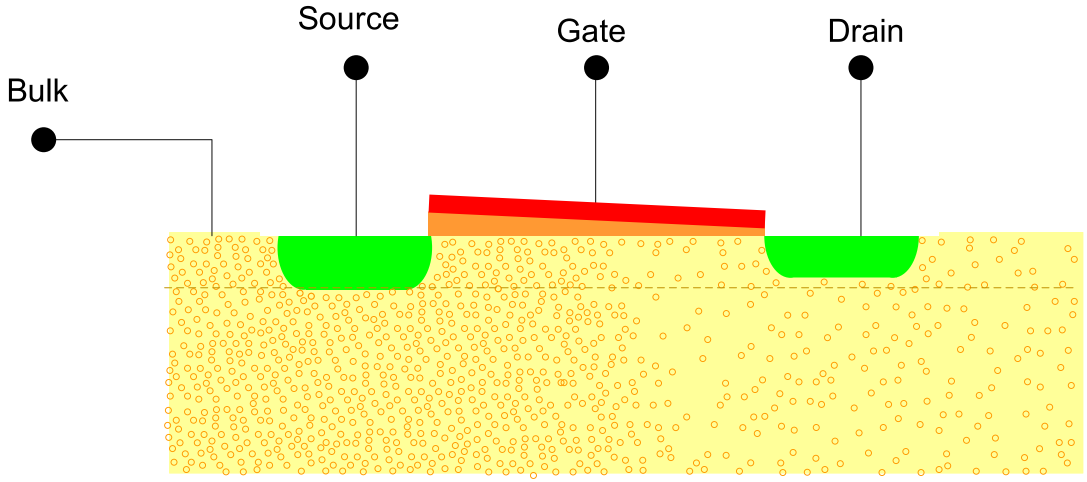
# Layout Issues for Matching Critical Components

- Matching is dominantly determined by local random variations and gradient effects – both of which are random variables at the design phase
- Mismatch induced by local random variations almost entirely determined by area allocated to matching-critical components
  - Good statistical analysis tools available for predicting mismatch induced by local random variations (Monte-Carlo analysis in SPECTRE)
  - Analytical formulations often (but not always) available for predicting effects of local random variations
  - At some resolution level, area required to maintain noise performance may dominate that required for matching due to local random variations
- Mismatch inducted by gradient effects strongly affected by layout
  - Gradient effects will usually dominate mismatch concerns if not managed
  - No good statistical analysis tools available for predicting mismatch induced by local random variations
  - Area allocation often plays no direct role in managing gradients though total span may play a role and may increase with area
  - Conventional-wisdom used to guide layout to manage gradient effects
  - With good layout techniques, gradient effects can usually be reduced below level of local random variations

# Local Random Variations and Gradients in MOS Devices



n-channel MOSFET

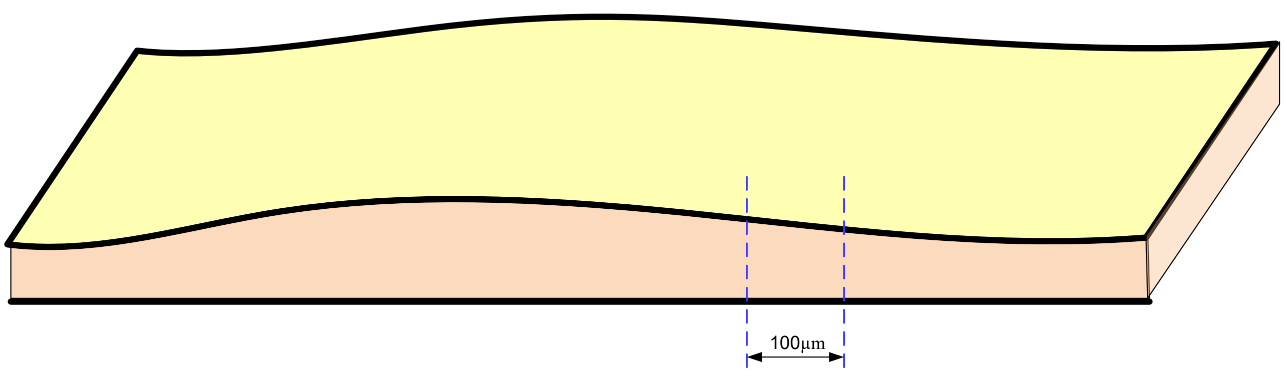


n-channel MOSFET

Impurity density or layer thicknesses vary linearly through the channel

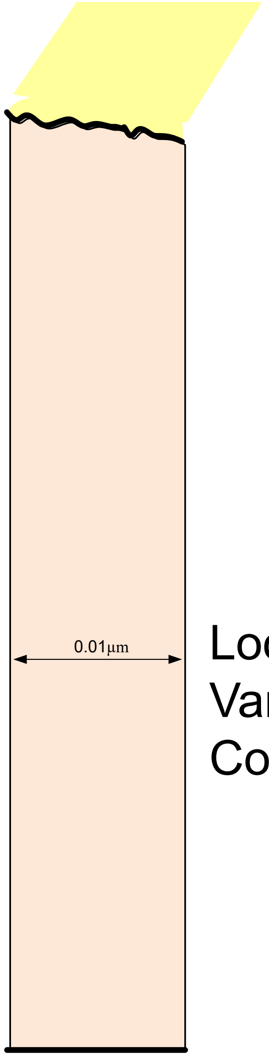
Model and design parameters vary throughout channel and  thus the corresponding equivalent lumped model parameters will vary from device to device

# Gradient and Local Random Effect



Gradient Effects : Locally Appear Linear

- Magnitude and Direction of Gradients are random
- Highly Correlated over Short Distances



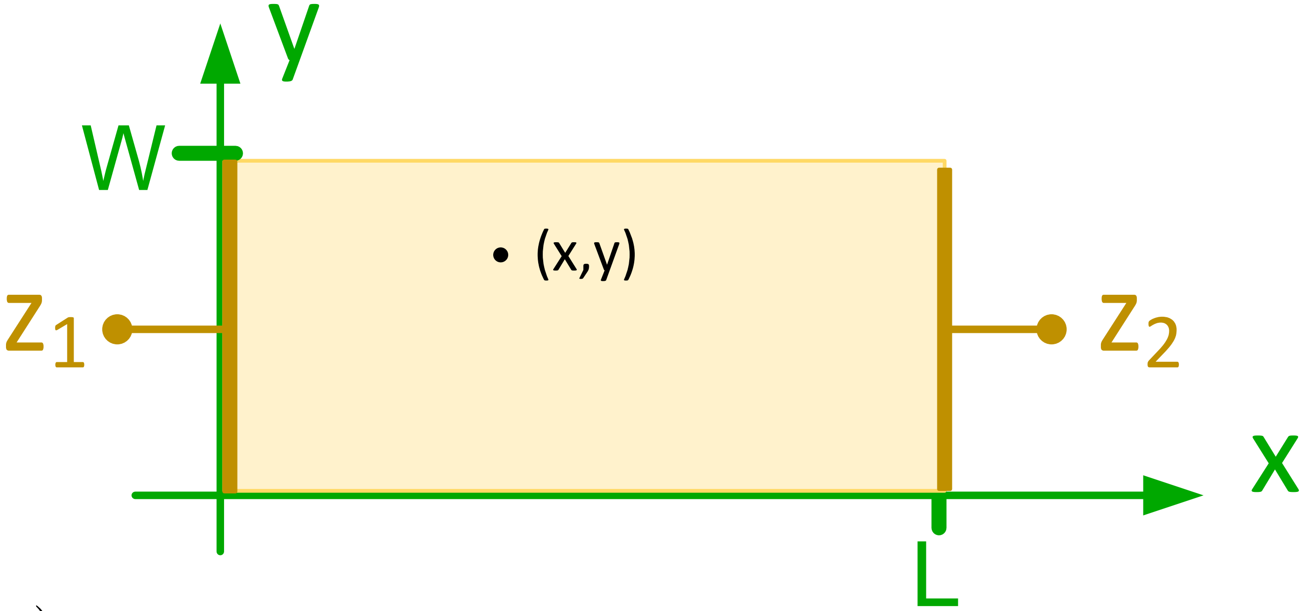
Local Random Effects :
Vary Locally With No
Correlation

- **Both contribute to mismatch**
- **Both are random variables**
- **If not managed, both can cause large mismatch effects**
- **Strategies for minimizing their effects are different**
- **Will refer to the local random effects as "random" and the random gradient effects as "gradient" effects**

From a previous lecture

# Resistor Characterization Concepts

Assume lithography is perfect, no gradient effects, and no contact resistance



$R_{\square}(x,y)$: Sheet resistance at (x,y)

Most authors assume:

$$R_{\square EQ} = \frac{\int_A R_{\square}(x,y)\,dxdy}{A} \qquad A=WL$$

$$R_{Z_1Z_2} = R_{\square EQ}\frac{L}{W}$$

We will make this same assumption

# Model Parameter Variation

Define p to be a process parameter that varies with lateral position throughout the region defined by the channel of the transistor.

Almost Theorem:

If p(x,y) varies throughout a two-dimensional region, then

$$\mathbf{p}_{\mathbf{EQ}} = \frac{\mathbf{1}}{\mathbf{A}} \int_{\mathbf{A}} \mathbf{p}(\mathbf{x},\mathbf{y})\,\mathbf{dxdy}$$

Parameters such at $V_T$, μ and $C_{OX}$ vary throughout a two-dimensional region

Local random variations introduce a random component in device model parameters which are uncorrelated but for ideally matched devices they are identically distributed

e.g. $V_{TEQi}=V_{TN}+V_{TR\,i}$

$V_{TRi}$ and $V_{TRj}$ due to local random variations are uncorrelated for i≠j but if ideally matched they are identically distributed

# Model Parameter Variation

Define p to be  a process parameter that varies with lateral position throughout the region defined by the channel of the transistor.

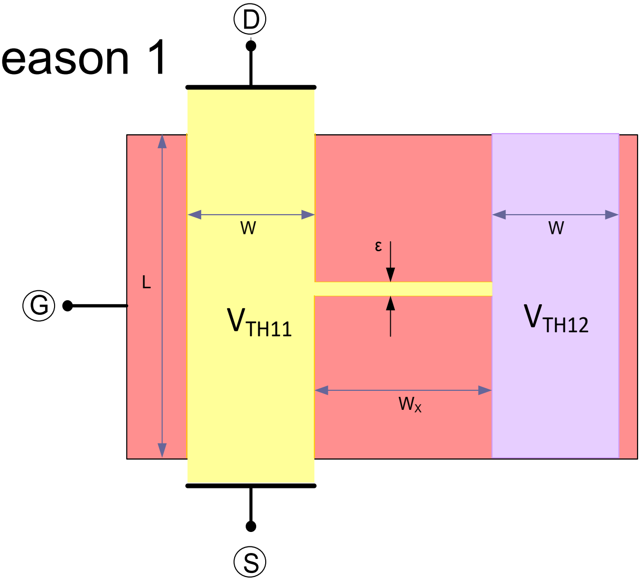
Almost Theorem:

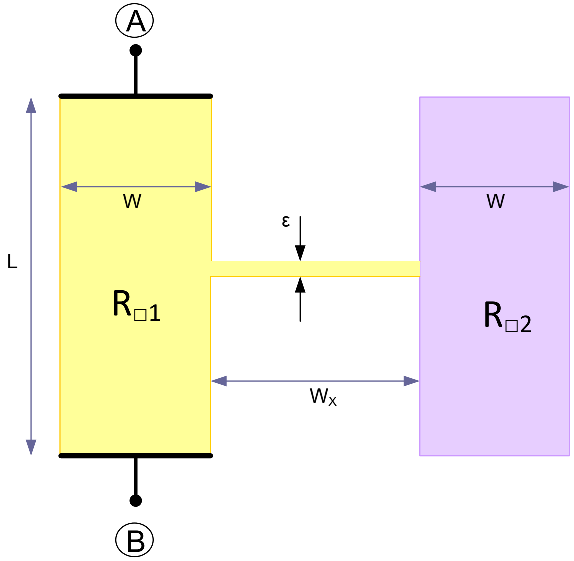
If p(x,y) varies throughout a two-dimensional region, then

$$p_{EQ} = \frac{1}{A}\int_A p(x,y)\,dx\,dy$$

Why almost?

Reason 1





Current densities dramatically different

# Model Parameter Variation

Define p to be a process parameter that varies with lateral position throughout the region defined by the channel of the transistor.

Almost Theorem:

If p(x,y) varies throughout a two-dimensional region, then

$$\mathbf{p_{EQ}} = \frac{\mathbf{1}}{\mathbf{A}} \int_{\mathbf{A}} \mathbf{p(x,y)dxdy}$$

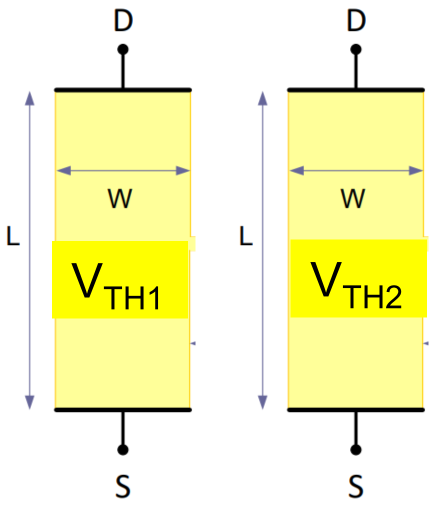
Why almost?

$$I_{D1} = \frac{\mu C_{OX} W}{2L}\left(V_{GS} - V_{TH1}\right)^2$$

$$I_{D2} = \frac{\mu C_{OX} W}{2L}\left(V_{GS} - V_{TH2}\right)^2$$

$$I_{DEQ} = \frac{\mu C_{OX} W}{2L}\left(V_{GS} - V_{THEQ}\right)^2$$

Reason 2

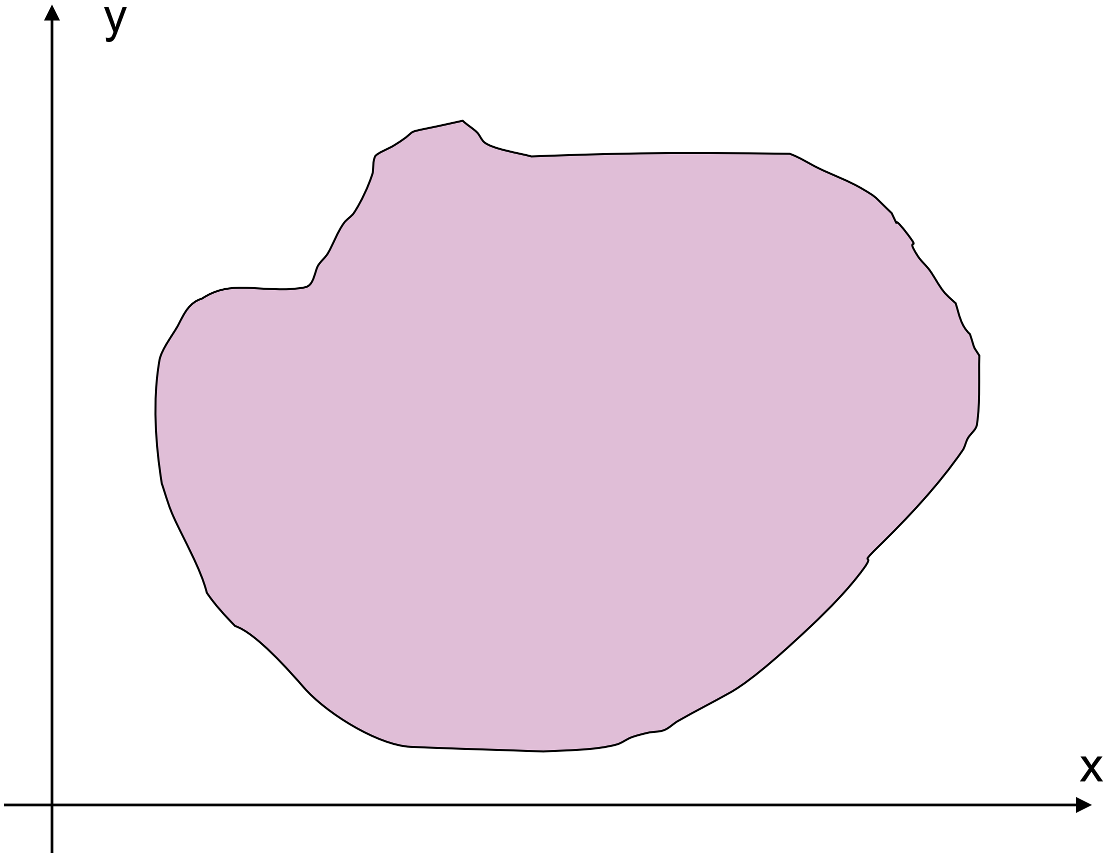


$$I_{DEQ} = \frac{\mu C_{OX} 2W}{2L}\left[V_{GS}^2 - V_{GS}\left(V_{TH1} + V_{TH2}\right) + \frac{V_{TH1}^2 + V_{TH2}^2}{2}\right]$$

$$I_{DEQ} = \frac{\mu C_{OX} W}{2L}\left[\left(V_{GS} - V_{TH1}\right)^2 + \left(V_{GS} - V_{TH2}\right)^2\right] \neq \frac{\mu C_{OX} W_{EQ}}{2L_{EQ}}\left(V_{GS} - \frac{V_{TH1} + V_{TH2}}{2}\right)^2$$

Models Inherently Different

# Model Parameter Variation



$$p_{EQ} = \frac{1}{A}\int_A p(x, y)\,dx\,dy$$

# Common Centroid Layouts

Define p to be a process parameter that varies linearly with lateral position throughout the region defined by the channel of the transistor.

Almost Theorem:

If p(x,y) varies linearly throughout a two-dimensional region, then

$$p_{EQ} = \frac{1}{A}\int_A p(x,y)dxdy$$

Gradient effects cause parameters such at $V_T$, μ and $C_{OX}$ to vary approximately linearly throughout a two-dimensional region as long at the “span” of the region is not too large

The direction and magnitude of gradients are random variables but are correlated and identical for closely-placed devices

# Common Centroid Layouts

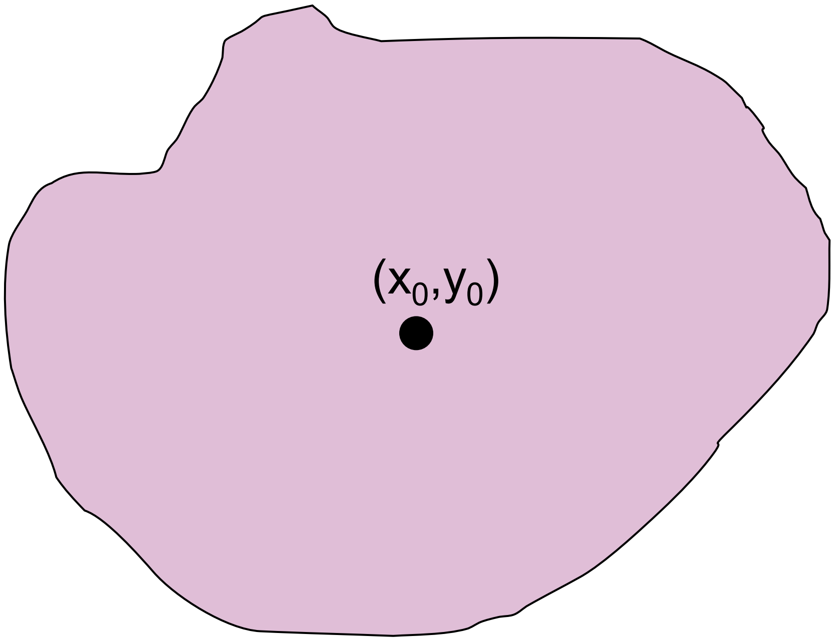
Almost Theorem:

If $p(x,y)$ varies linearly throughout a two-dimensional region, then $p_{EQ}=p(x_0.y_0)$ where $x_0,y_0$ is the geometric centroid to the region.

If a parameter varies linearly throughout a two-dimensional region, it is said to have a linear gradient.

Many parameters have a dominantly linear gradient over rather small regions but large enough to encompass layouts where devices are ideally matched

# Common Centroid Layouts



$(x_0,y_0)$ is geometric centroid

$$\mathbf{p_{EQ} = \frac{1}{A}\int_A p(x,y)dxdy}$$

If ρ(x,y) varies linearly in any direction, then the theorem states

$$p_{EQ} = \frac{1}{A}\int_A p(x,y)dxdy = p(x_0,y_0)$$

# Common Centroid Layouts

Definition: A layout of two devices is termed a common-centroid layout if both devices have the same geometric centroid

Almost Theorem:

If p(x,y) varies linearly throughout a two-dimensional region, then if two devices have the same centroid, the lateral-variable parameters are matched !

Note: This is true independent of the magnitude and direction of the gradient!

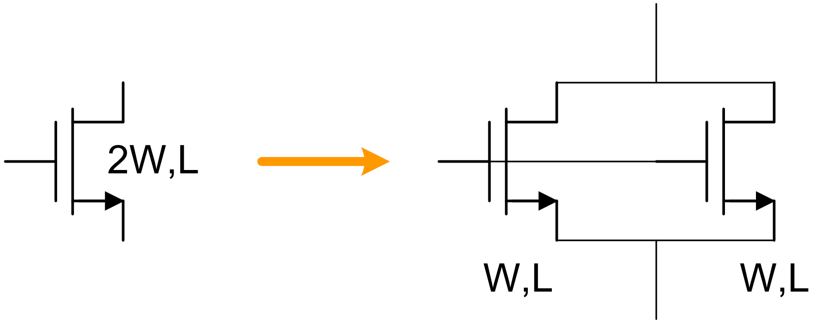
Almost Theorem:

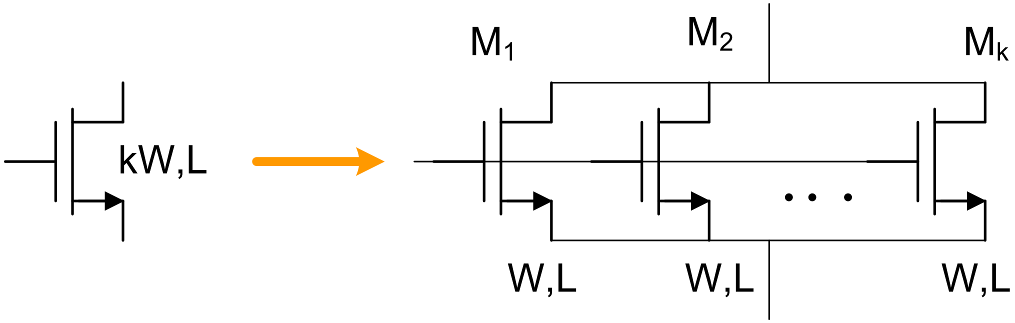
If a common-centroid layout is used for the matching-critical part of an operational amplifier, the lateral-variable parameters (e.g. $V_{TH}$, μ, $C_{OX}$) will introduce no mismatch!

Common-centroid layouts almost always used for matching-critical components to eliminate linear gradients of critical parameters !

But local random variations will still affect matching even if gradient effects are eliminated

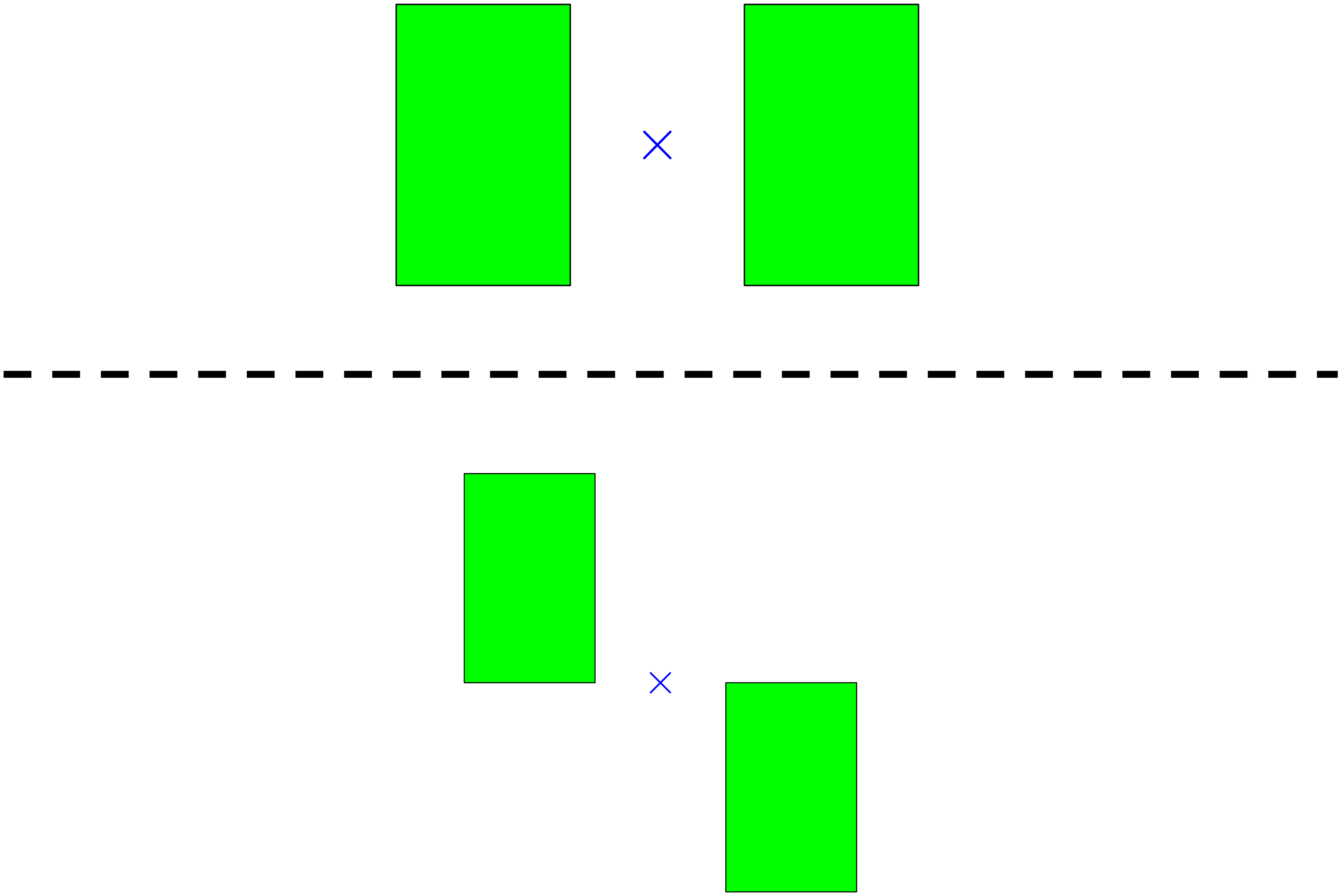
# Recall parallel combinations of transistors equivalent to a single transistor of appropriate W,L



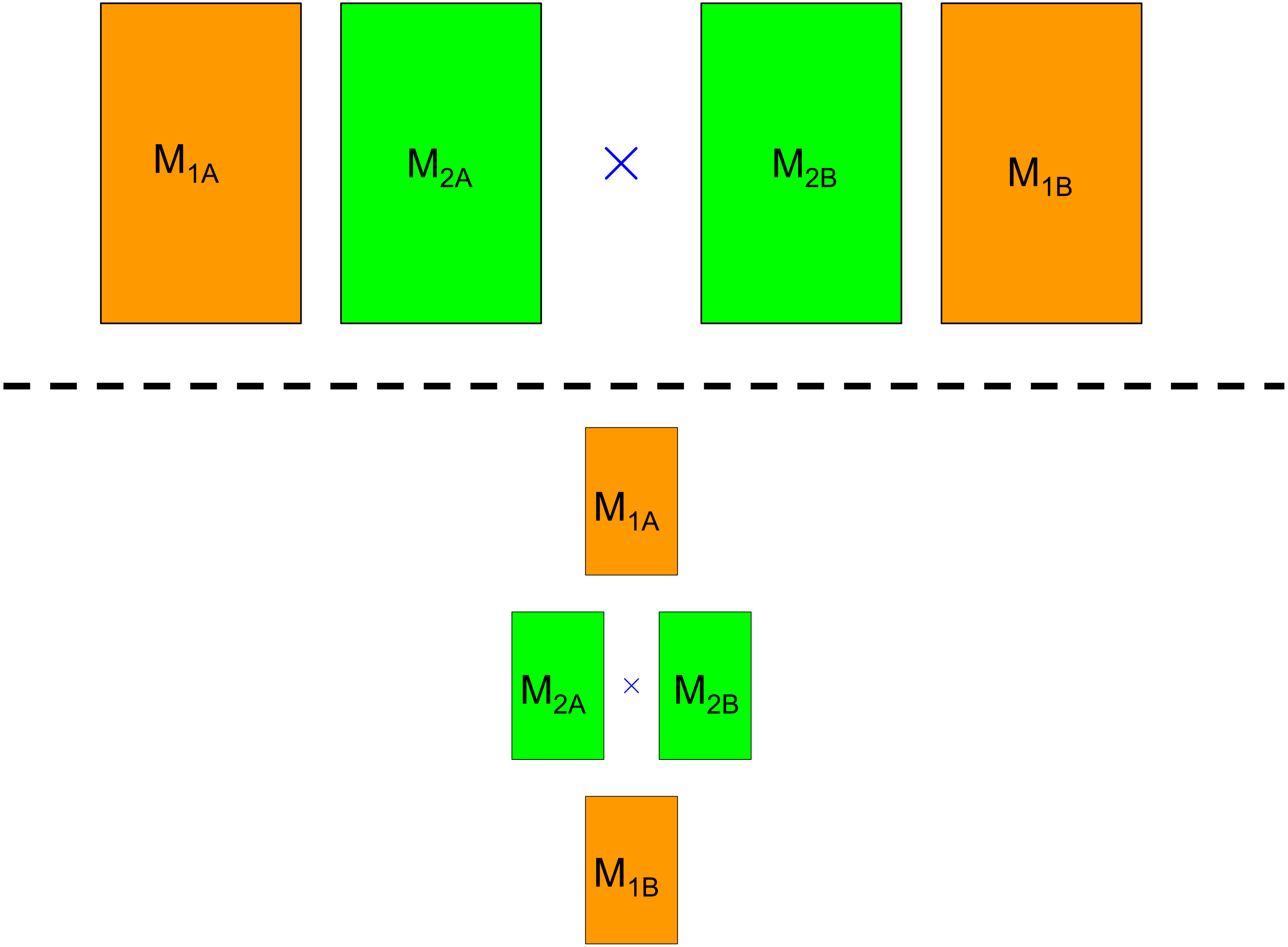


# Centroids of Segmented Geometries

× Denotes Geometric Centroid

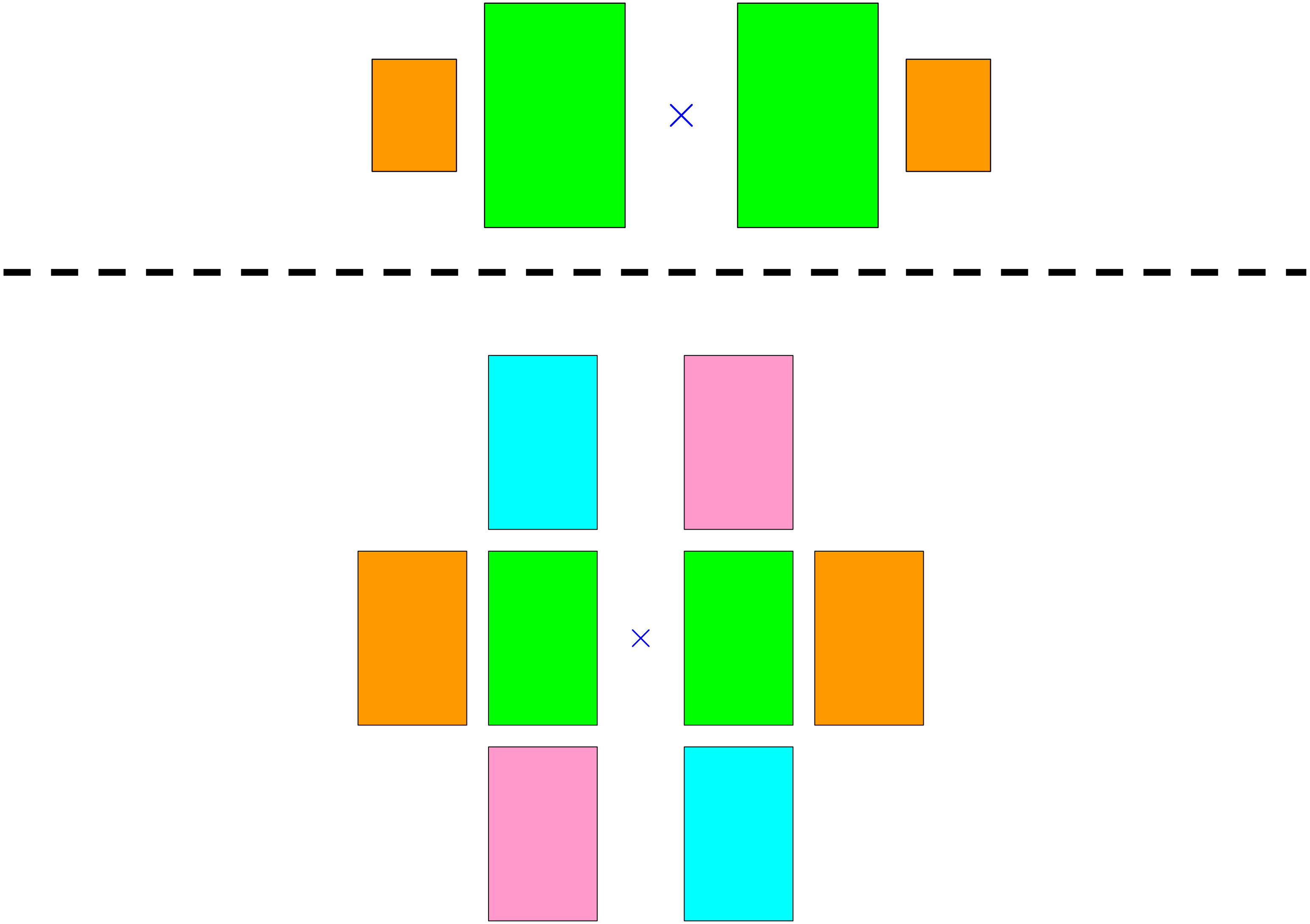


# Common Centroid of Multiple Segmented Geometries

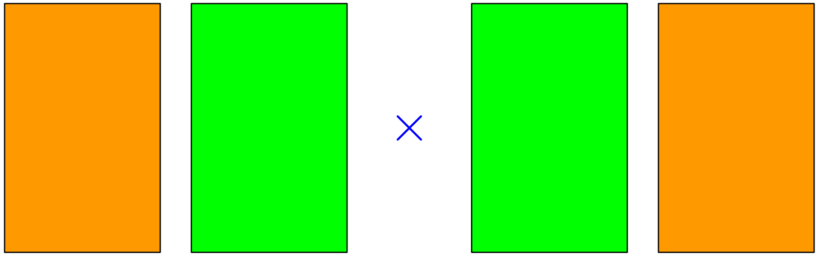


If these are layouts of gates of two transistors with two segments, $M_1$ and $M_2$ have common centroids. They are thus termed common-centroid layouts

# Common Centroid of Multiple Segmented Geometries



# Common Centroid Layouts



Common centroid layouts widely (almost always) used where matching of devices or components is critical because these layouts will cancel all first-order gradient effects

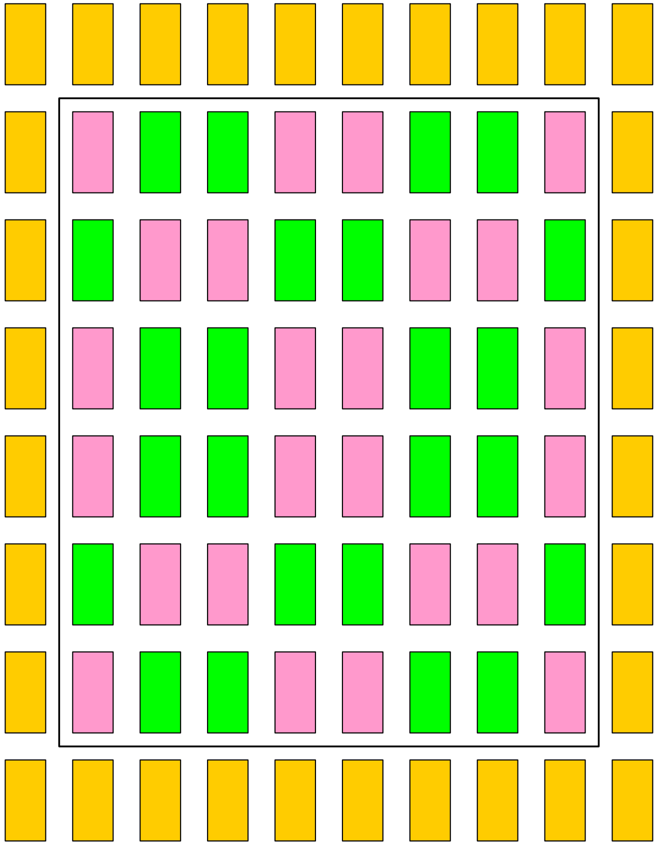
Applies to resistors, capacitors, transistors and other components

Always orient all devices in the same way

Keep common centroid for interconnects, diffusions, and all features

Often dummy devices placed on periphery to improve matching !

# Common Centroid Layout Surrounded by Dummy Devices



More than one ring of dummy devices may be required

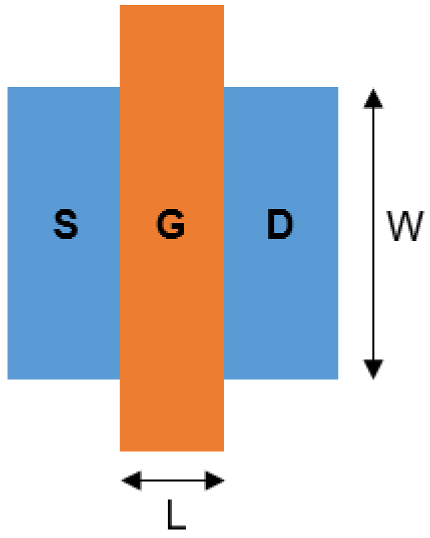
Dummy devices may be used for other purposes as well

e.g. bypass capacitors for capacitor arrays or binary-weighted LSB devices for segmented structures

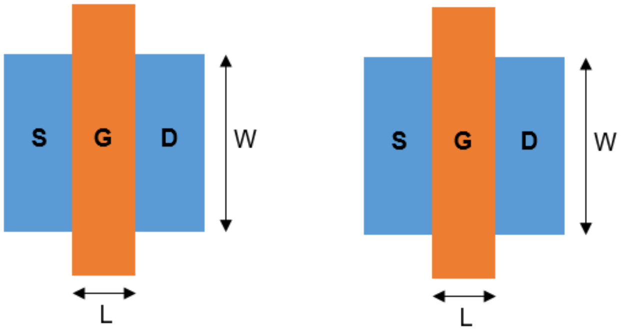
# Fingers and Multipliers

- Multiple fingers use shared diffusions
- Multipliers refer to multiple copies of transistors with individual drains and sources

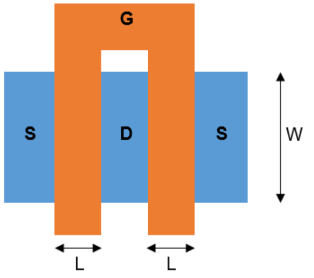
Important to match orientation if overall device matching is required



Multiplier = 2

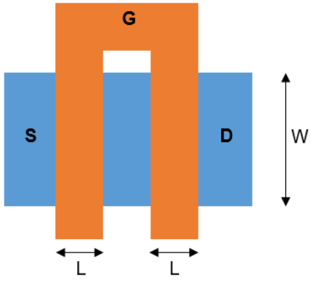


Fingers = 2



$L_{eff}=L$, $W_{eff}=2W$

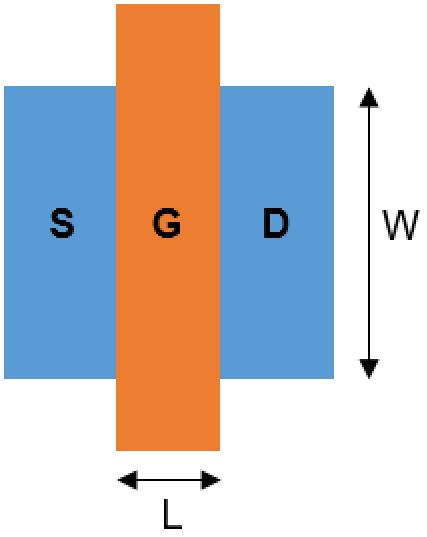
Fingers = 2



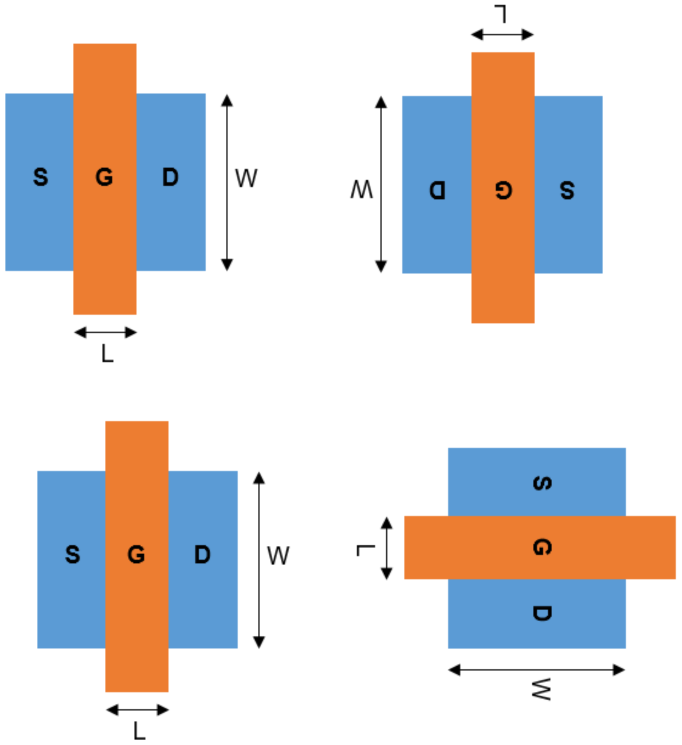
$L_{eff}=2L$, $W_{eff}=W$

https://electronics.stackexchange.com/questions/246463/multiple-fingers-vs-single-finger-layout-mosfet-transistor

# Fingers and Multipliers



Alternate Orientations



If matching is important, orientations should be identical

https://electronics.stackexchange.com/questions/246463/multiple-fingers-vs-single-finger-layout-mosfet-transistor

End of Lecture 26